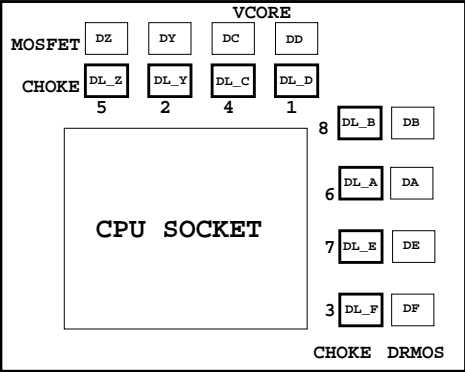


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	DVI / DP
15	R_USB3 / HDMI
16	PLX8605
17	PCI EXPRESS*1 SLOTS X3
18	Dual BIOS
19	CT9570 Audio
20	Audio Connect
21	Audio Power
22	IR3580 PWM
23	IR3598-VCORE
24	IR3570_DDR PWM
25	IR3598-DDR
26	DISCRETE POWER I
27	DISCRETE POWER II
28	I/O ITE8620
29	FP,F_USB,BZ
30	USB DAC-UP , PS2
31	ATX POWER
32	RST, PWR, CLR_CMOS, 80 PORT
33	LAN E2201
34	INTEL I217

35	RENEASAS USB3 HUB-1
36	RENEASAS USB3 HUB-1
37	F_USB3.0 , SATA EXPRESS
38	IT8790
39	FAN CTRL
40	PCIEx16(x8) REFCLK
41	PCI EXPRESS*16_2 SLOT
42	PCI EXPRESS X16 SWITCH_2
43	PCI EXPRESS*8_2 SLOT
44	PCI EXPRESS*16_1 SLOT
45	PCI EXPRESS X16 SWITCH_1
46	PCI EXPRESS*8_1 SLOT
47	PEX8747S UPSTREAM & MISC
48	PEX8747S DOWNSTREAM SLOTS
49	PEX8747S STRAP & CPLD INTF
50	PEX8747S POWER
51	PEX8747 POWER DESIGN
52	Marvell 9172 1
53	Marvell 9172 2
54	TABLE LIST



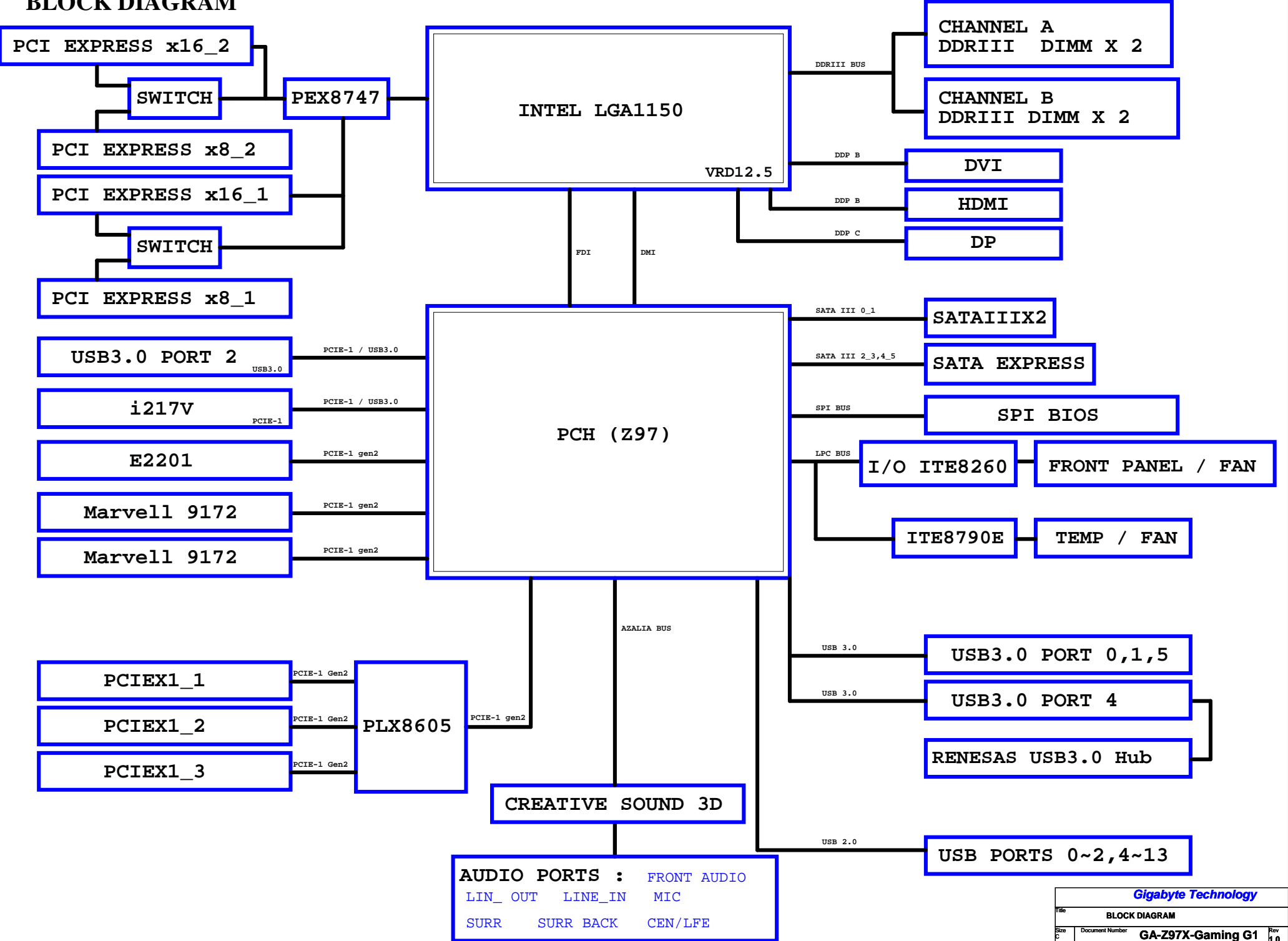
Component value change history

[illegible][illegible]

Circuit or PCB layout change

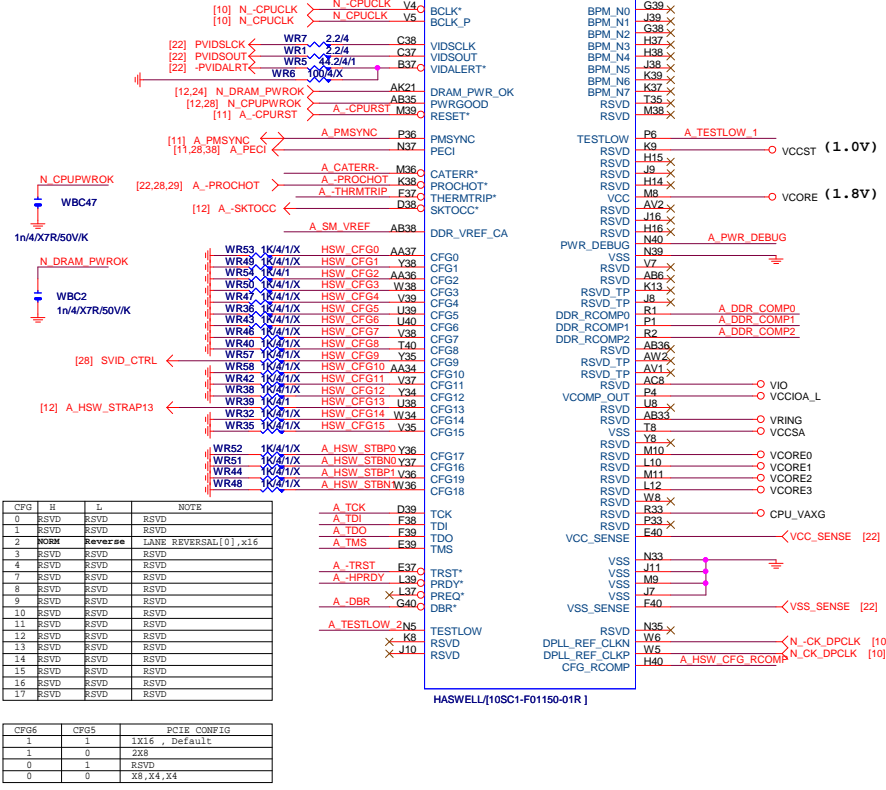
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BLOCK DIAGRAM



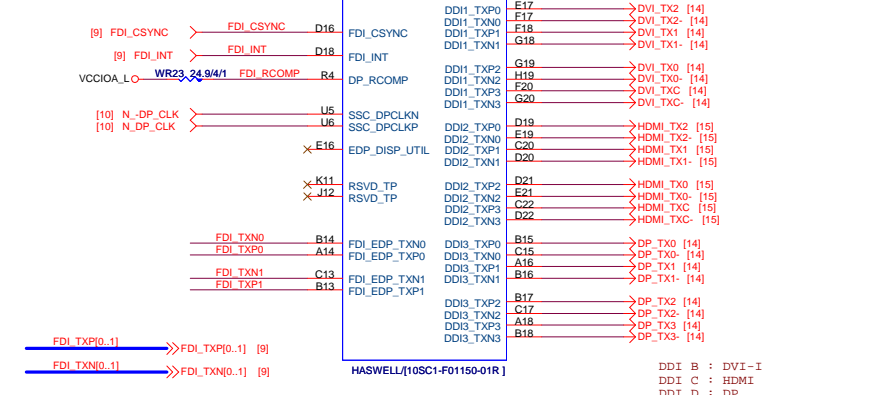
LGA1150

(E)



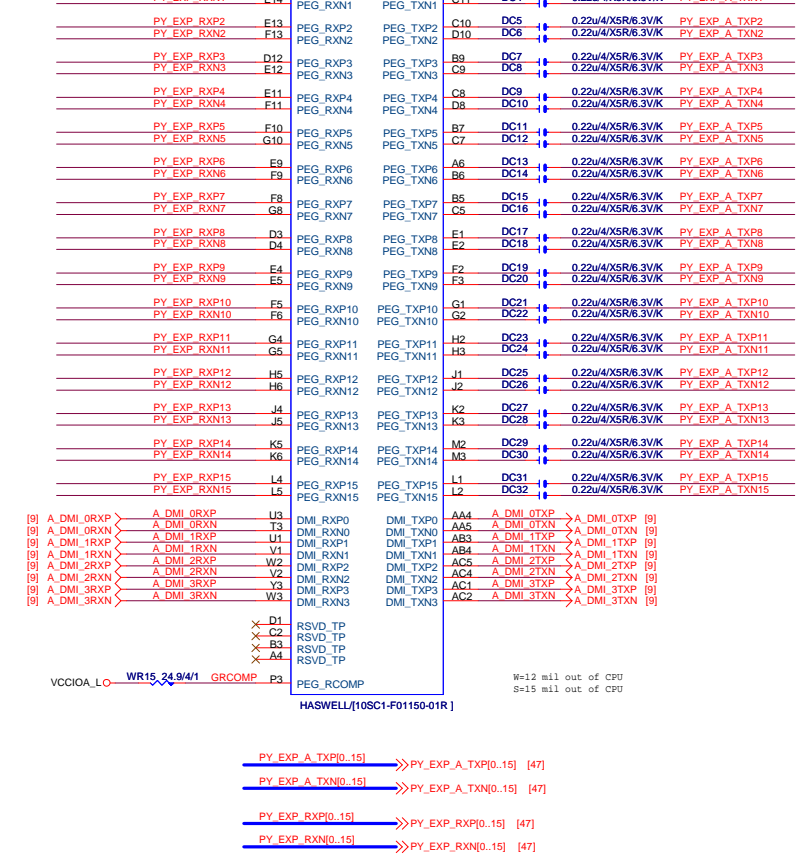
LGA1150

(D)

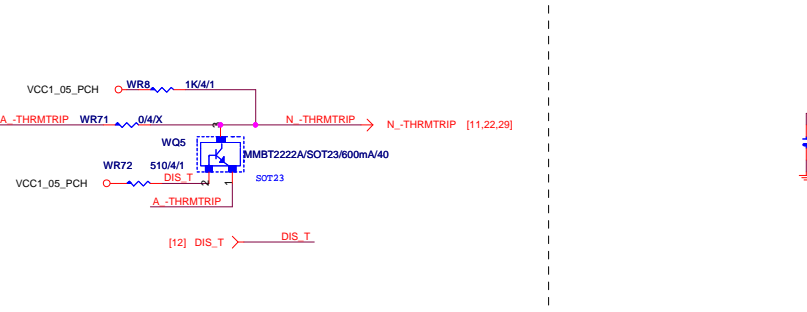


LGA1150

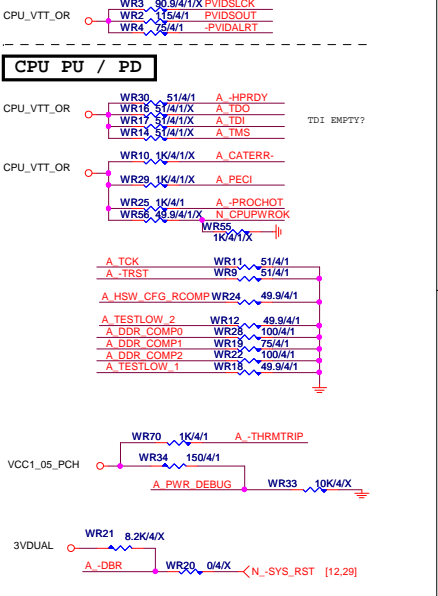
(C)



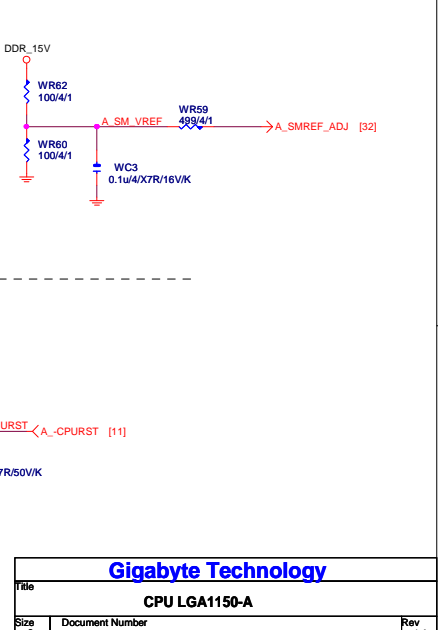
THRMTRIP DISABLE



CPU SVID



SM REF



LGA1150A

MAAA0	AU13	DDR0_M0	DDR0_D00	AD38	MDA0
MAAA1	AV16	DDR0_M1	DDR0_D01	AD39	MDA1
MAAA2	AU16	DDR0_M2	DDR0_D02	AF38	MDA2
MAAA3	AU17	DDR0_M3	DDR0_D03	AE39	MDA3
MAAA4	AU17	DDR0_M4	DDR0_D04	AD37	MDA4
MAAA5	AW18	DDR0_M5	DDR0_D05	AD40	MDA5
MAAA6	AV17	DDR0_M6	DDR0_D06	AE37	MDA6
MAAA7	AT18	DDR0_M7	DDR0_D07	AF40	MDA7
MAAA8	AU18	DDR0_M8	DDR0_D08	AH40	MDA9
MAAA9	AT19	DDR0_M9	DDR0_D09	AH39	MDA13
MAAA10	AW11	DDR0_M10	DDR0_D10	AK38	MDA10
MAAA11	AV19	DDR0_M11	DDR0_D11	AK39	MDA11
MAAA12	AU19	DDR0_M12	DDR0_D12	AH37	MDA12
MAAA13	AT10	DDR0_M13	DDR0_D13	AH38	MDA8
MAAA14	AT20	DDR0_M14	DDR0_D14	AK37	MDA14
MAAA15	AU21	DDR0_M15	DDR0_D15	AK40	MDA15
MODT_A0	AW10	DDR0_ODT0	DDR0_ODT0	AM40	MDA17
MODT_A1	AY8	DDR0_ODT1	DDR0_ODT1	AM39	MDA21
MODT_A2	AW9	DDR0_ODT2	DDR0_ODT2	AP38	MDA18
MODT_A3	AU8	DDR0_ODT3	DDR0_ODT3	AP39	MDA19

AW33	DDR0_ECC0	DDR0_D022	AP40	MDA23
AW33	DDR0_ECC1	DDR0_D023	AP40	MDA23
AW33	DDR0_ECC2	DDR0_D024	AP40	MDA23
AW33	DDR0_ECC3	DDR0_D025	AP40	MDA23
AW33	DDR0_ECC4	DDR0_D026	AP40	MDA23
AW33	DDR0_ECC5	DDR0_D027	AP40	MDA23
AW33	DDR0_ECC6	DDR0_D028	AP40	MDA23
AW33	DDR0_ECC7	DDR0_D029	AP40	MDA23

[7] SBA0	←	SBA0	AV12	DDR0_BA0	DDR0_D030
[7] SBA1	←	SBA1	AV11	DDR0_BA1	DDR0_D031
[7] SBA2	←	SBA2	AT21	DDR0_BA2	DDR0_D032
[7] CKEA0	←	CKEA0	AV22	DDR0_CKE0	DDR0_D033
[7] CKEA1	←	CKEA1	AT23	DDR0_CKE1	DDR0_D034
[7] CKEA2	←	CKEA2	AU22	DDR0_CKE2	DDR0_D035
[7] CKEA3	←	CKEA3	AU23	DDR0_CKE3	DDR0_D036

[7] -CSA0	←	-CSA0	AU14	DDR0_CS_N0	DDR0_D037
[7] -CSA1	←	-CSA1	AV9	DDR0_CS_N1	DDR0_D038
[7] -CSA2	←	-CSA2	AU10	DDR0_CS_N2	DDR0_D039
[7] -CSA3	←	-CSA3	AW8	DDR0_CS_N3	DDR0_D040

[7] DCLKA0	←	DCLKA0	AY15	DDR0_CLK_P0	DDR0_D041
[7] -DCLKA0	←	-DCLKA0	AY16	DDR0_CLK_N0	DDR0_D042
[7] DCLKA1	←	DCLKA1	AY15	DDR0_CLK_P1	DDR0_D043
[7] -DCLKA1	←	-DCLKA1	AY16	DDR0_CLK_N1	DDR0_D044
[7] DCLKA2	←	DCLKA2	AY14	DDR0_CLK_P2	DDR0_D045
[7] -DCLKA2	←	-DCLKA2	AY14	DDR0_CLK_N2	DDR0_D046
[7] DCLKA3	←	DCLKA3	AY13	DDR0_CLK_P3	DDR0_D047
[7] -DCLKA3	←	-DCLKA3	AY13	DDR0_CLK_N3	DDR0_D048

AW12	RSVD	DDR0_D049	AN1	MDA47
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[7] -SRASA	←	-SRASA	AU12C	DDR0_RAS*	DDR0_D050
[7] -SWEA	←	-SWEA	AU11C	DDR0_WE*	DDR0_D051

AW20C	RSVD	DDR0_D052	AN39	DOSA2
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AW27C	RSVD	DDR0_D053	AV36	DOSA3
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[7] -SCASA	←	-SCASA	AU9C	DDR0_CAS*	DDR0_D054
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[7,8] -DDR3_RST	←	WR61	0.1u/4X7R/16V/K/X	AK22C	DDR_RESET*
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HASWELL[10SC1-F01150-01R]

LGA1150B

MAAB0	AL19	DDR1_M0	DDR1_D00	AE34	MDB0
MAAB1	AK23	DDR1_M1	DDR1_D01	AE35	MDB1
MAAB2	AM22	DDR1_M2	DDR1_D02	AG35	MDB2
MAAB3	AM23	DDR1_M3	DDR1_D03	AH35	MDB3
MAAB4	AP23	DDR1_M4	DDR1_D04	AD34	MDB4
MAAB5	AL23	DDR1_M5	DDR1_D05	AD35	MDB5
MAAB6	AY24	DDR1_M6	DDR1_D06	AH34	MDB6
MAAB7	AV25	DDR1_M7	DDR1_D07	AH34	MDB7
MAAB8	AW25	DDR1_M8	DDR1_D08	AL34	MDB8
MAAB9	AP18	DDR1_M9	DDR1_D09	AL35	MDB9
MAAB10	AY25	DDR1_M10	DDR1_D10	AK31	MDB10
MAAB11	AY26	DDR1_M11	DDR1_D11	AL31	MDB11
MAAB12	AR15	DDR1_M12	DDR1_D12	AK34	MDB12
MAAB13	AV27	DDR1_M13	DDR1_D13	AK32	MDB14
MAAB14	AV27	DDR1_M14	DDR1_D14	AL32	MDB15
MAAB15	AV28	DDR1_M15	DDR1_D15	AN34	MDB17
MODT_B0	AM17	DDR1_ODT0	DDR1_ODT0	AP34	MDB19
MODT_B1	AL16	DDR1_ODT1	DDR1_ODT1	AN31	MDB19
MODT_B2	AM16	DDR1_ODT2	DDR1_ODT2	AP31	MDB23
MODT_B3	AK15	DDR1_ODT3	DDR1_ODT3	AN32	MDB20

AM26	DDR1_ECC0	DDR1_D022	AP32	MDB22
AM26	DDR1_ECC1	DDR1_D023	AP32	MDB22
AM26	DDR1_ECC2	DDR1_D024	AP32	MDB22
AM26	DDR1_ECC3	DDR1_D025	AP32	MDB22
AM26	DDR1_ECC4	DDR1_D026	AP32	MDB22
AM26	DDR1_ECC5	DDR1_D027	AP32	MDB22
AM26	DDR1_ECC6	DDR1_D028	AP32	MDB22
AM26	DDR1_ECC7	DDR1_D029	AP32	MDB22

[8] SBA0	←	SBA0	AK17	DDR1_BA0	DDR1_D031
[8] SBA1	←	SBA1	AL18	DDR1_BA1	DDR1_D032
[8] SBA2	←	SBA2	AW28	DDR1_BA2	DDR1_D033
[8] CKEB0	←	CKEB0	AW29	DDR1_CKE0	DDR1_D034
[8] CKEB1	←	CKEB1	AY29	DDR1_CKE1	DDR1_D035
[8] CKEB2	←	CKEB2	AU28	DDR1_CKE2	DDR1_D036
[8] CKEB3	←	CKEB3	AU29	DDR1_CKE3	DDR1_D037

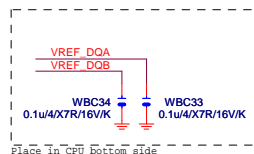
[8] -CSB0	←	-CSB0	AP17	DDR1_CS_N0	DDR1_D038
[8] -CSB1	←	-CSB1	AN15	DDR1_CS_N1	DDR1_D039
[8] -CSB2	←	-CSB2	AN17	DDR1_CS_N2	DDR1_D040
[8] -CSB3	←	-CSB3	AL15	DDR1_CS_N3	DDR1_D041

[8] DCLKB0	←	DCLKB0	AM20	DDR1_CLK_P0	DDR1_D042
[8] -DCLKB0	←	-DCLKB0	AM21	DDR1_CLK_N0	DDR1_D043
[8] DCLKB1	←	DCLKB1	AP22	DDR1_CLK_P1	DDR1_D044
[8] -DCLKB1	←	-DCLKB1	AP21	DDR1_CLK_N1	DDR1_D045

[8] DCLKB2	←	DCLKB2	AN20	DDR1_CLK_P2	DDR1_D046
[8] -DCLKB2	←	-DCLKB2	AN21	DDR1_CLK_N2	DDR1_D047
[8] DCLKB3	←	DCLKB3	AP19	DDR1_CLK_P3	DDR1_D048
[8] -DCLKB3	←	-DCLKB3	AP20	DDR1_CLK_N3	DDR1_D049

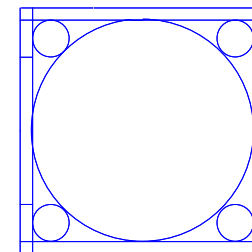
[8] -SCASB	←	-SCASB	AP16C	DDR1_CAS*	DDR1_D050
[8] -SRASB	←	-SRASB	AM18C	DDR1_RAS*	DDR1_D051
[8] -SWEB	←	-SWEB	AK16C	DDR1_WE*	DDR1_D052

[7] VREF_DQA	←	AB39	DDR_VREF_DQ0	DDR_VREF_DQ0	DDR1_D053
[8] VREF_DQB	←	AB40	DDR_VREF_DQ1	DDR_VREF_DQ1	DDR1_D054



Place In CPU bottom side

HASWELL[10SC1-F01150-01R]

LGA1150
ILM_BP1156/BKNI[12KRC-0F0001-61R]

Need check the new CPU ME

DDR BUS

[7] MODT_A[0..3]	←	MODT_A[0..3]
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[8] MODT_B[0..3]	←	MODT_B[0..3]
------------------	---	--------------

[7] MDA[0..63]	←	MDA[0..63]
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[8] MDB[0..63]	←	MDB[0..63]
----------------	---	------------

[7] DQSA[0..7]	←	DQSA[0..7]
----------------	---	------------

[7] -DQSA[0..7]	←	-DQSA[0..7]
-----------------	---	-------------

[7] MAAA[0..15]	←	MAAA[0..15]
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[8] MAAB[0..15]	←	MAAB[0..15]
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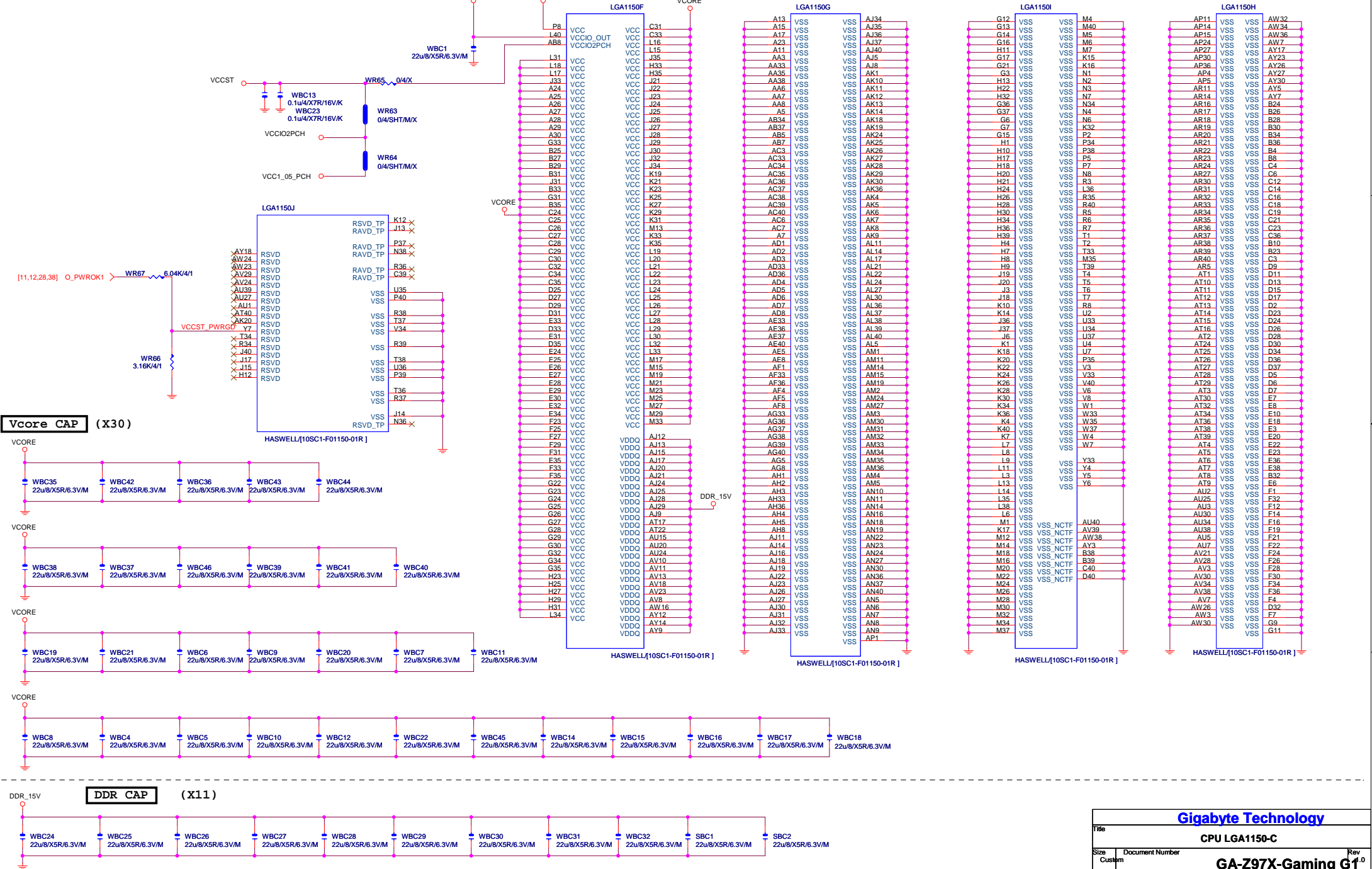
[8] DQSB[0..7]	←	DQSB[0..7]
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[8] -DQSB[0..7]	←	-DQSB[0..7]
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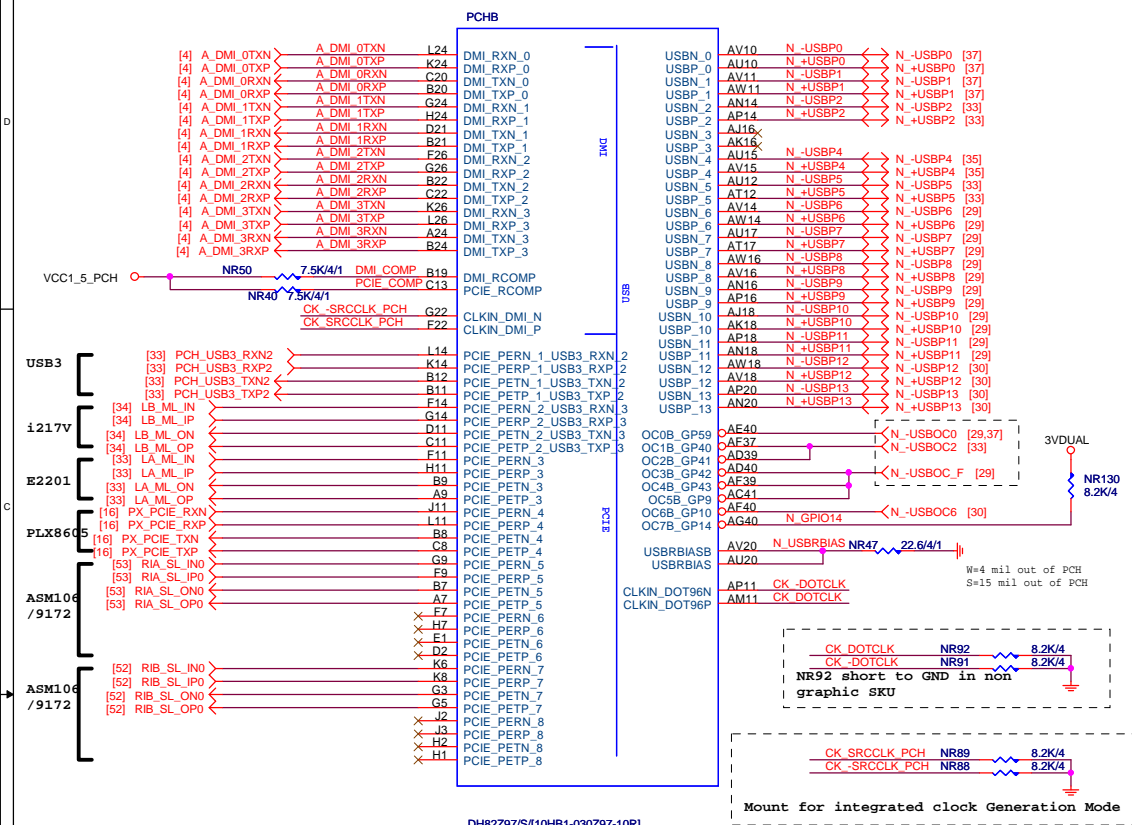
Gigabyte Technology

Title		CPU LGA1150-B	
Size	Document Number	Rev	
Custom	GA-Z97X-Gaming G1.0	1.0	
Date:	Wednesday, March 05, 2014	Sheet	5 of 54

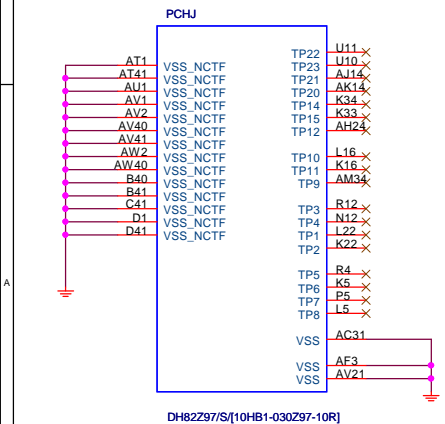
LGA1150 (J,F,G,I,H)



PCH (B)



PCH (J)



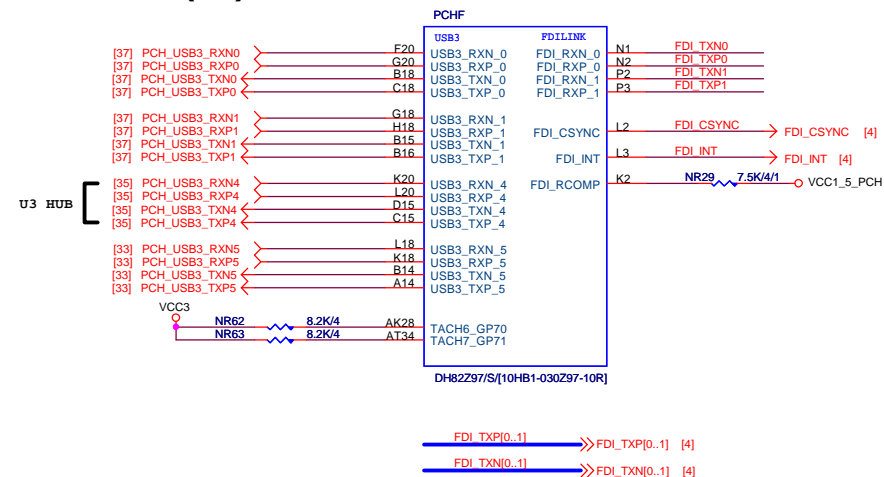
USB	TABLE
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OC[3:0]# for Device 29 (ports 0-7)

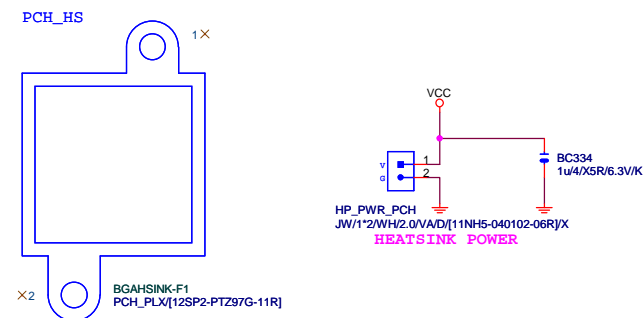
OC[7:4]# for Device 26 (ports 8-13)

USB3	00 01	04	05	F_USB1	F_USB2
USB2	00 01	04	05	02 03	06 07
OC	OC0	D720210_Hub	D720210_Hub	OC_F	

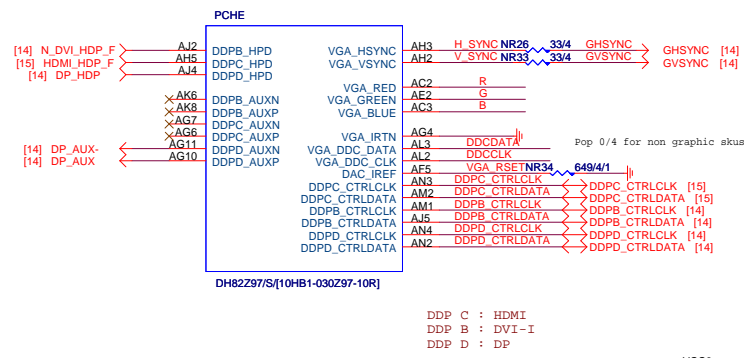
PCH (F)



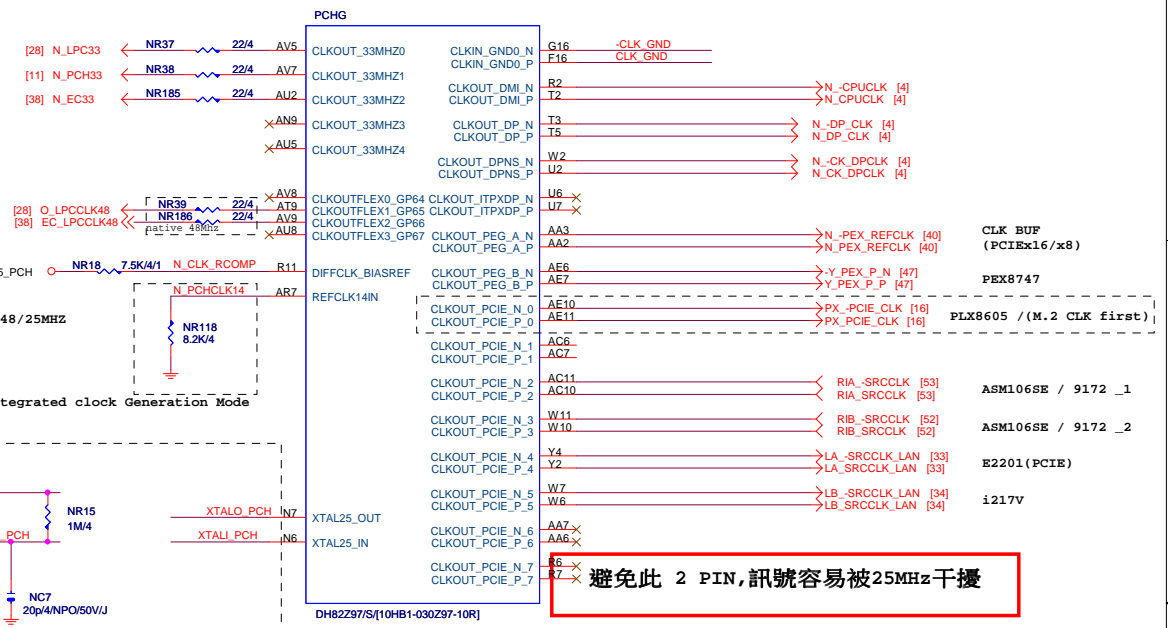
PCH Heatsink



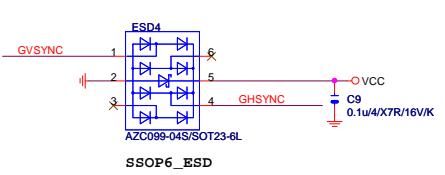
PCH (E)



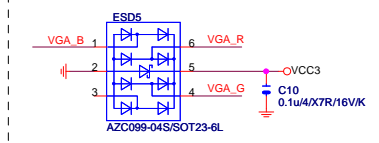
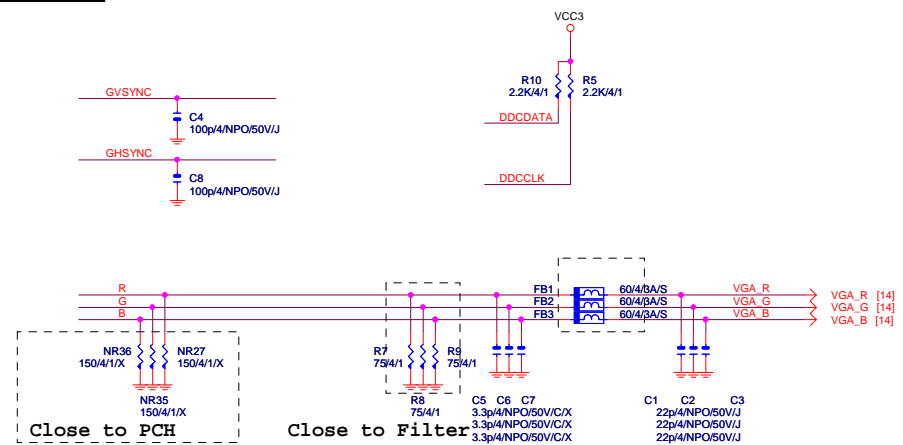
PCH (G)



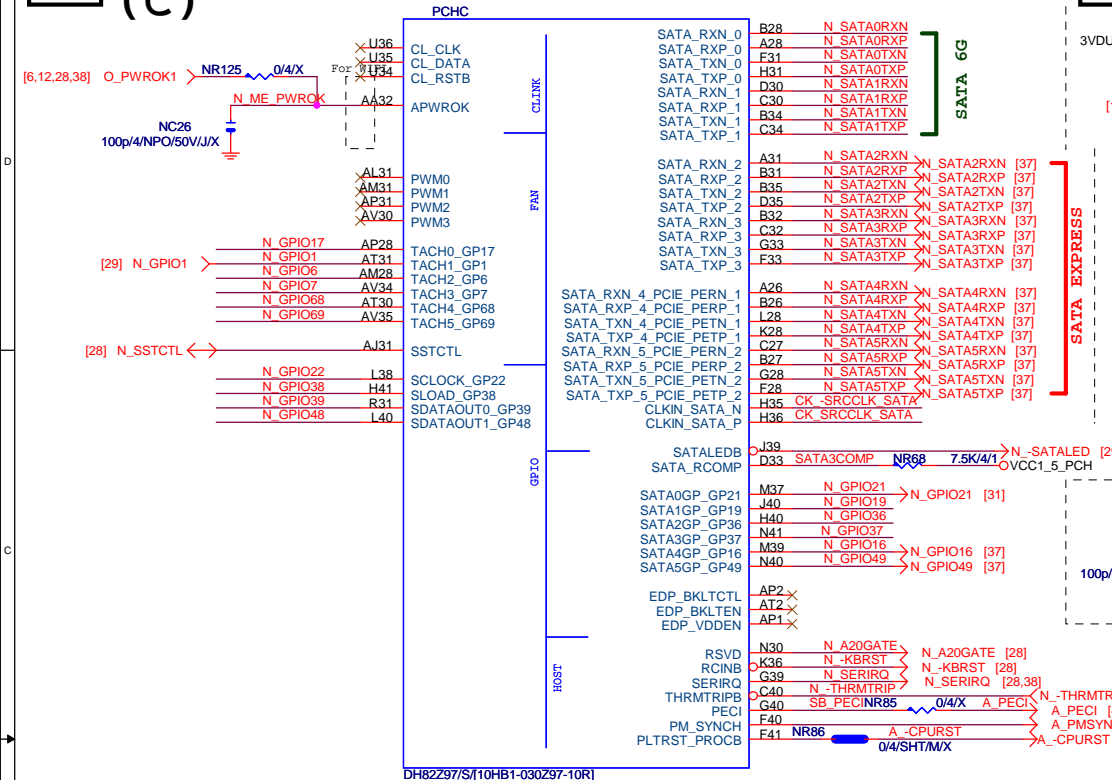
VGA ESD



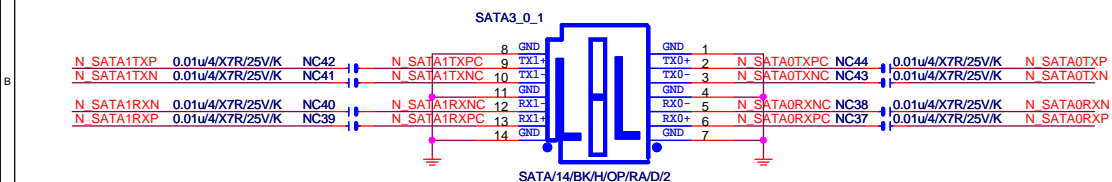
VGA DDC



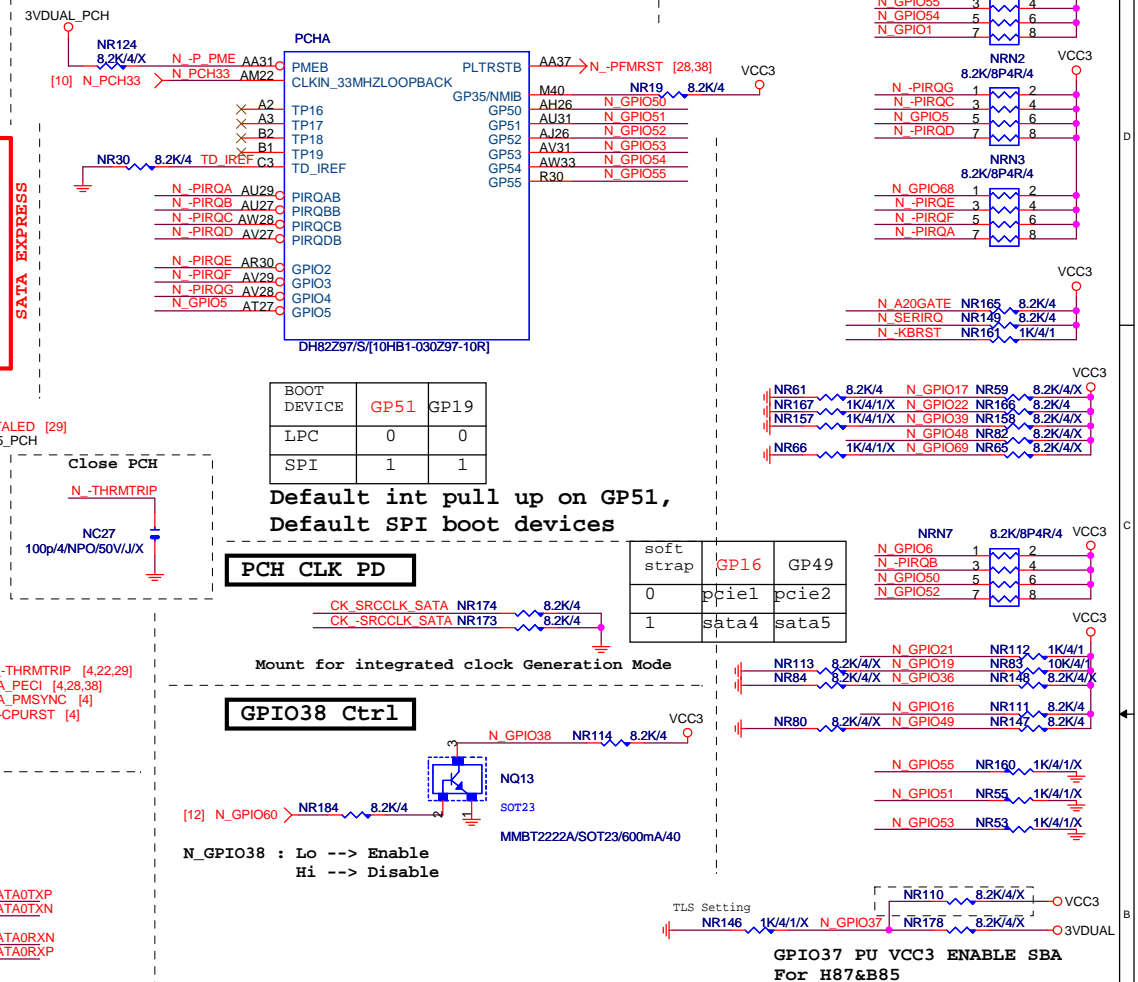
(c)



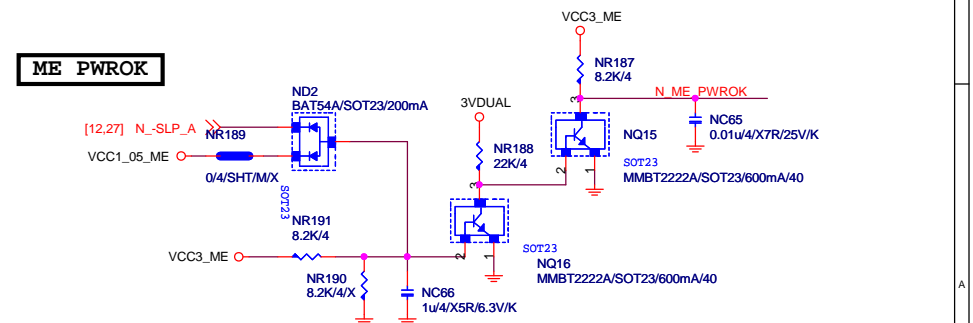
SATA3 CONNECTOR



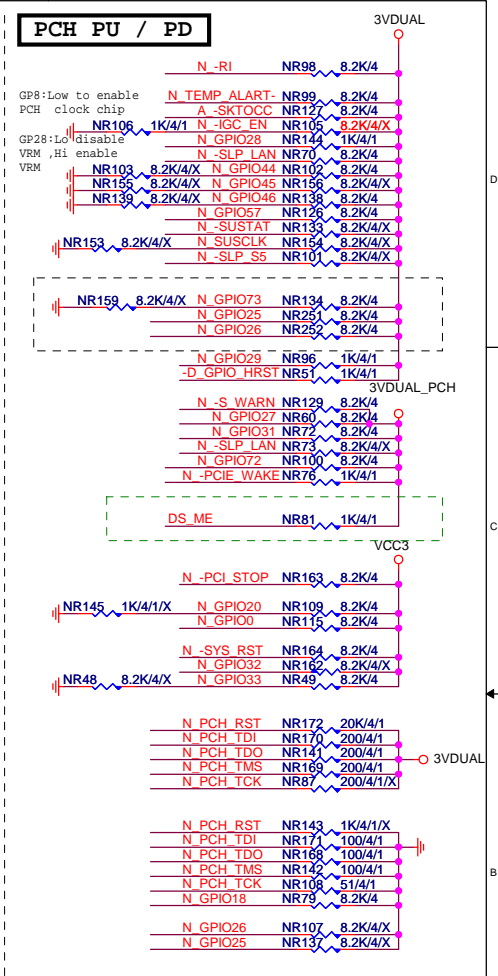
PCH (A)



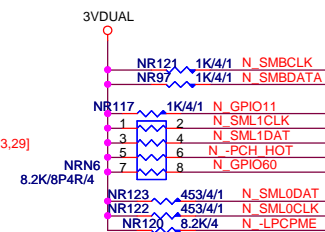
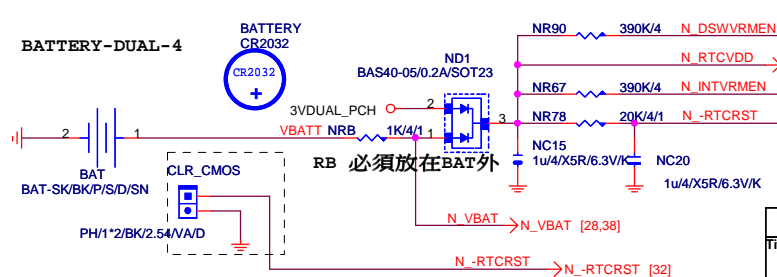
ME PWROK



(D)

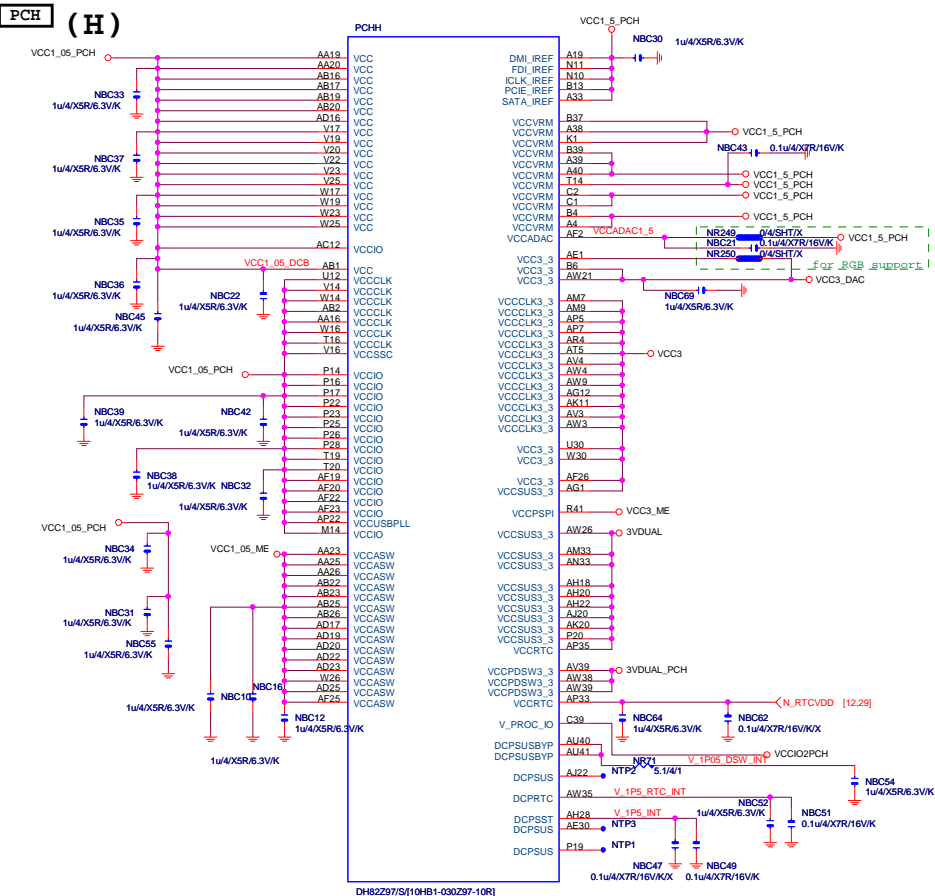


CLR	CMOS
1	1
0	0

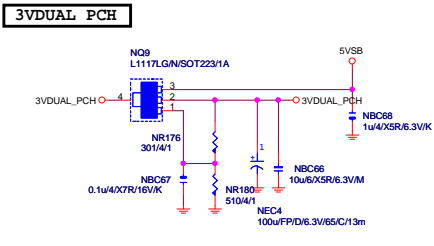


Title			
PCH GPIO , CTRL , AUDIO			
Size B	Document Number		Rev 1.0
GA-Z97X-Gaming G1			
Date:	Wednesday, March 05, 2014	Sheet 12 of 54	

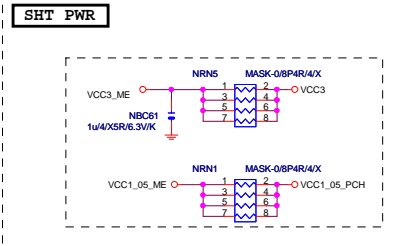
PCH (H)



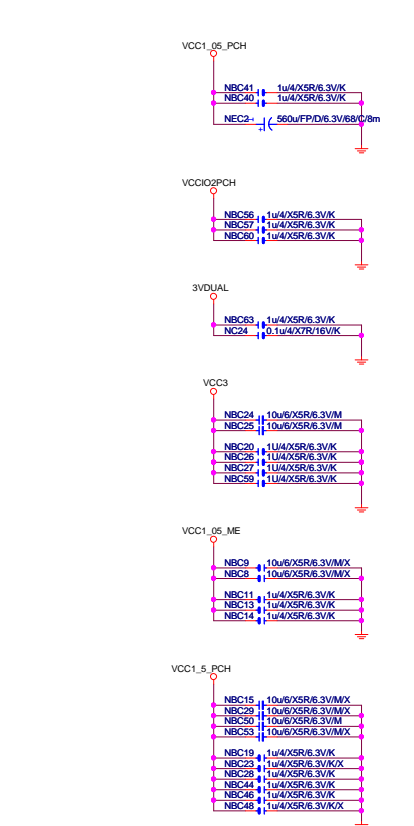
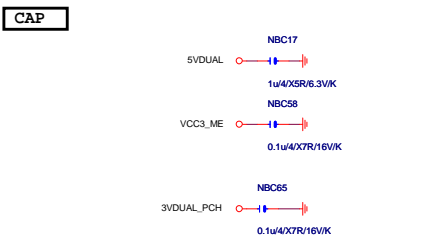
3VDUAL PCH



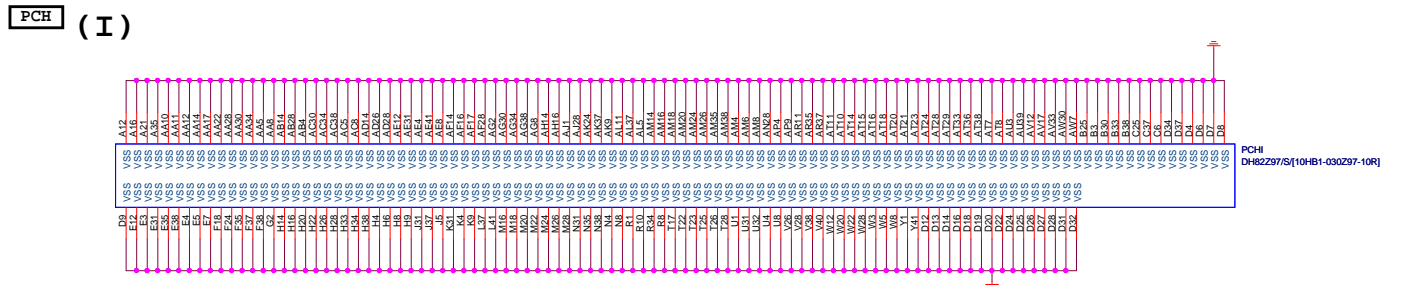
SHT PWR

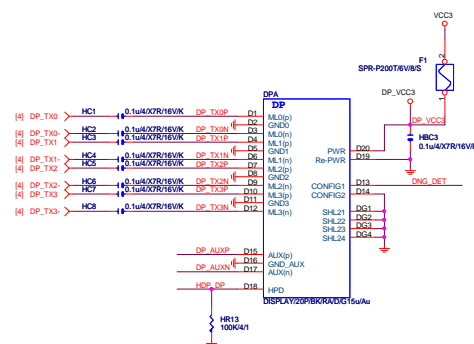
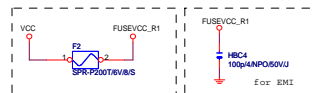
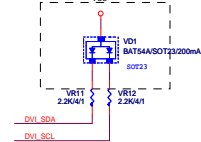


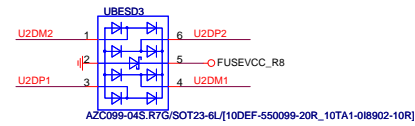
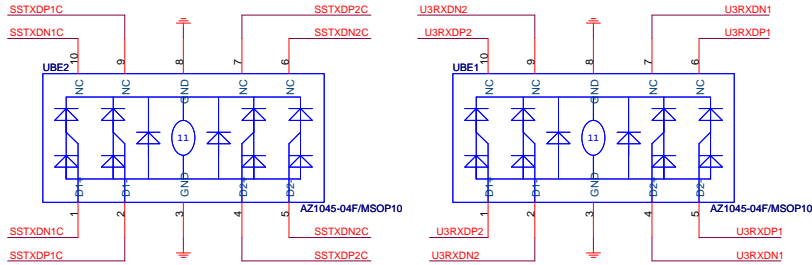
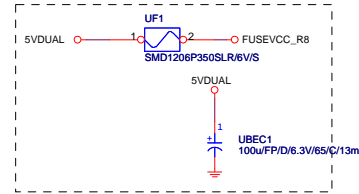
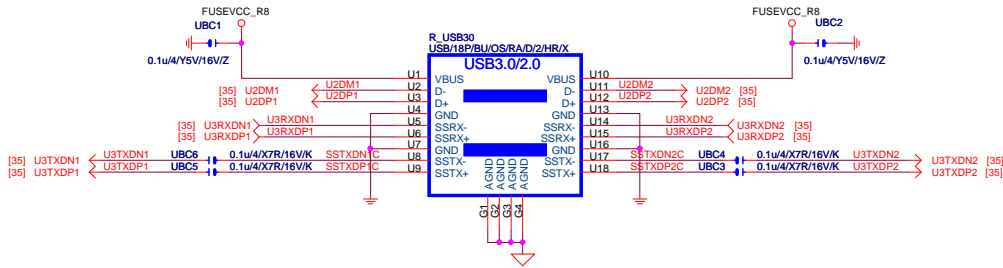
CAP



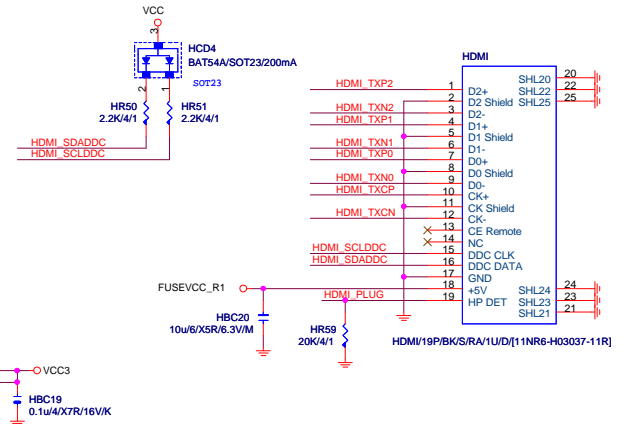
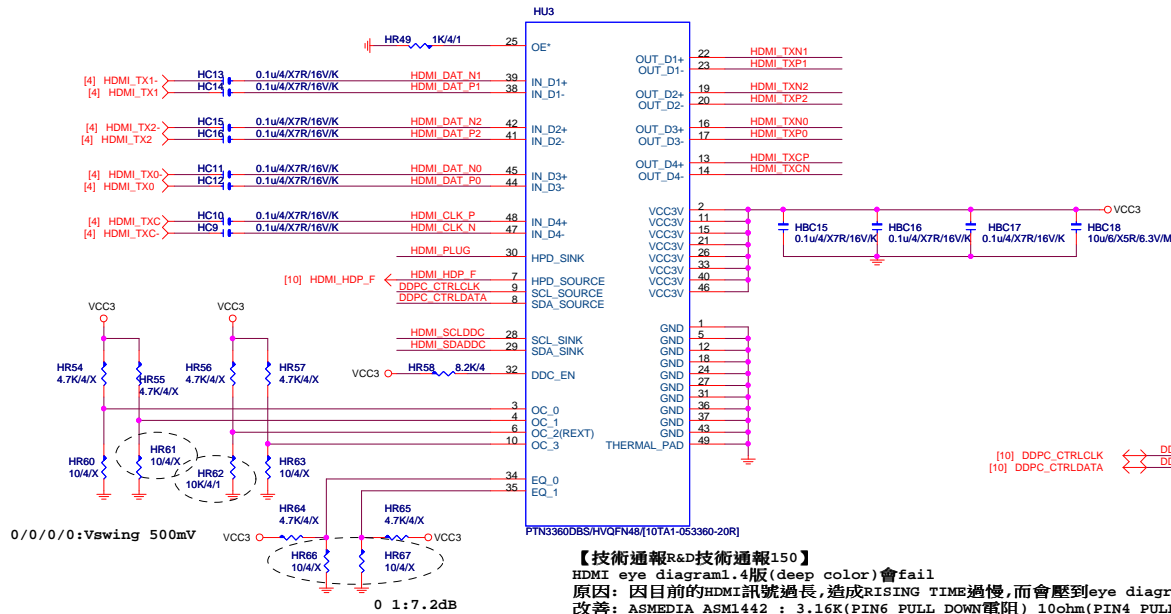
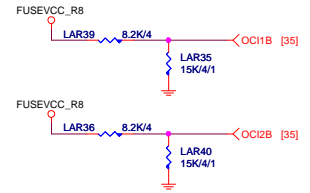
PCH (I





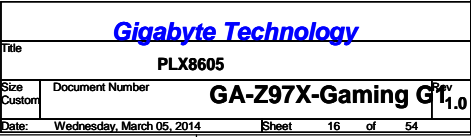


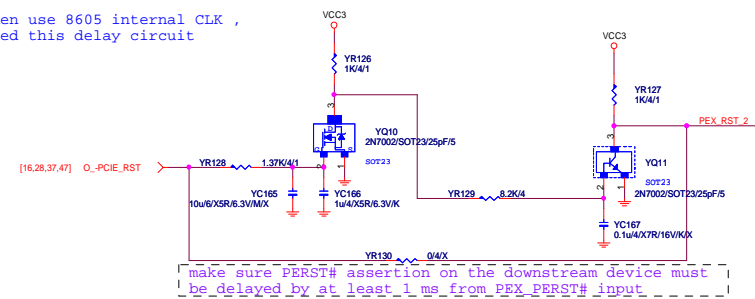
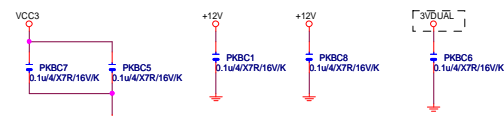
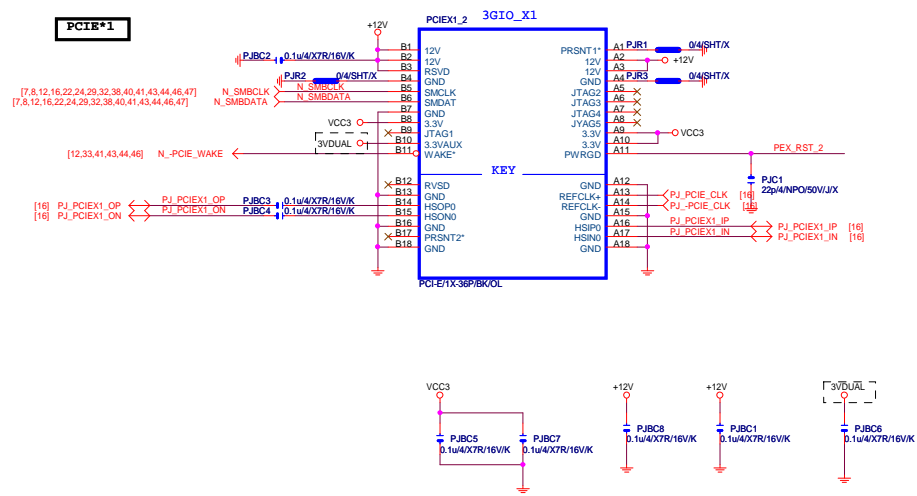
Close to connector



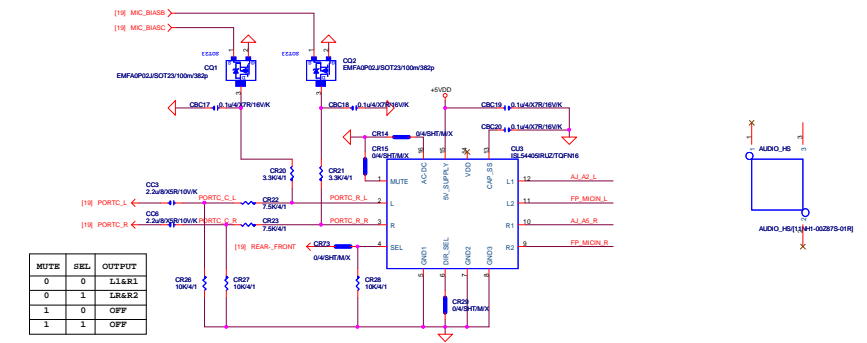
【技術通報R&D技術通報150】
HDMI eye diagram 1.4版(deep color)會fail
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

Gigabyte Technology			
File		USB3 / HDMI	
Size	Document Number	GA-Z97X-Gaming G1	
Date	Wednesday, March 05, 2014	Sheet	15 of 54

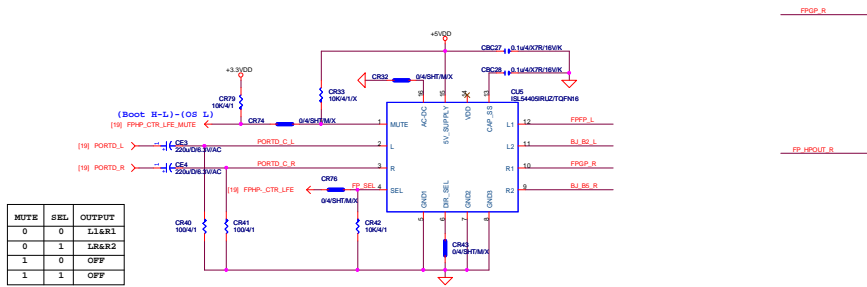




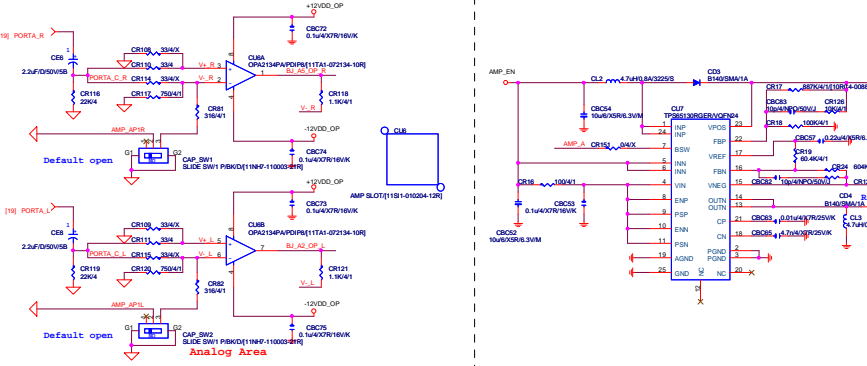
Rear MIC & FP MIC



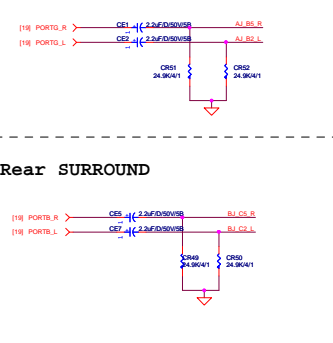
Rear CEN/LFE & FP HP-Out



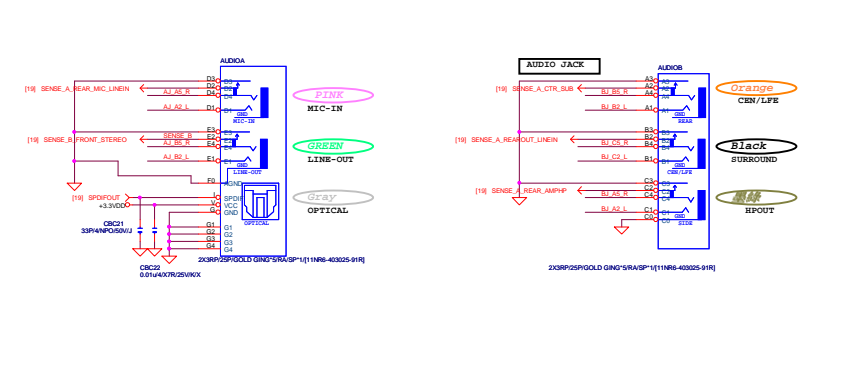
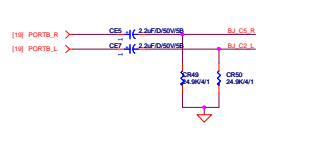
AMPLIFIED



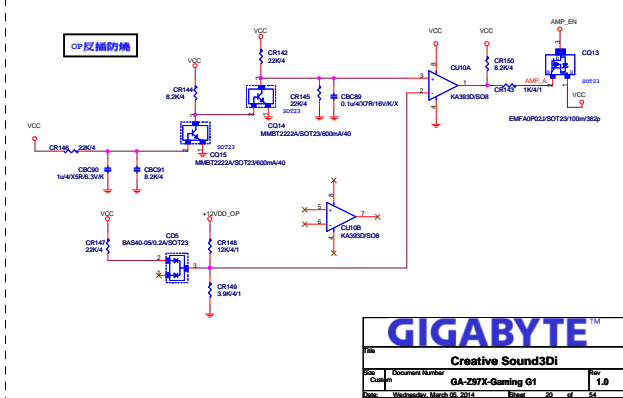
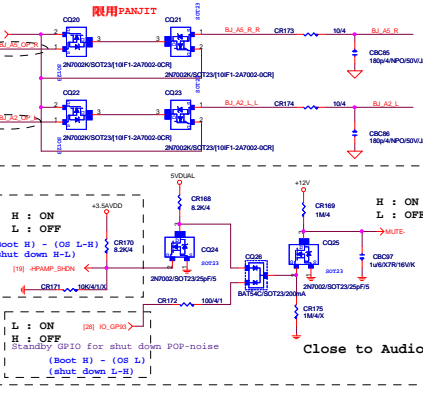
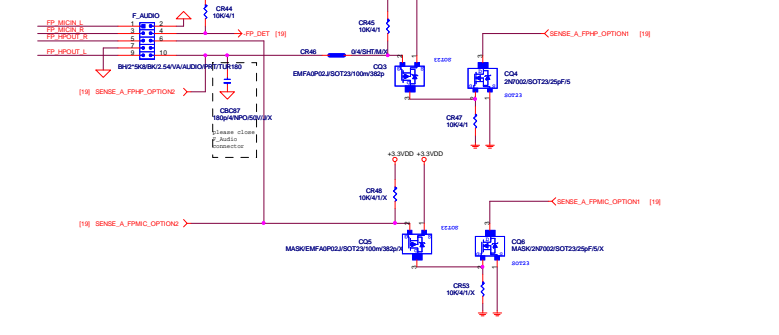
Line-Out

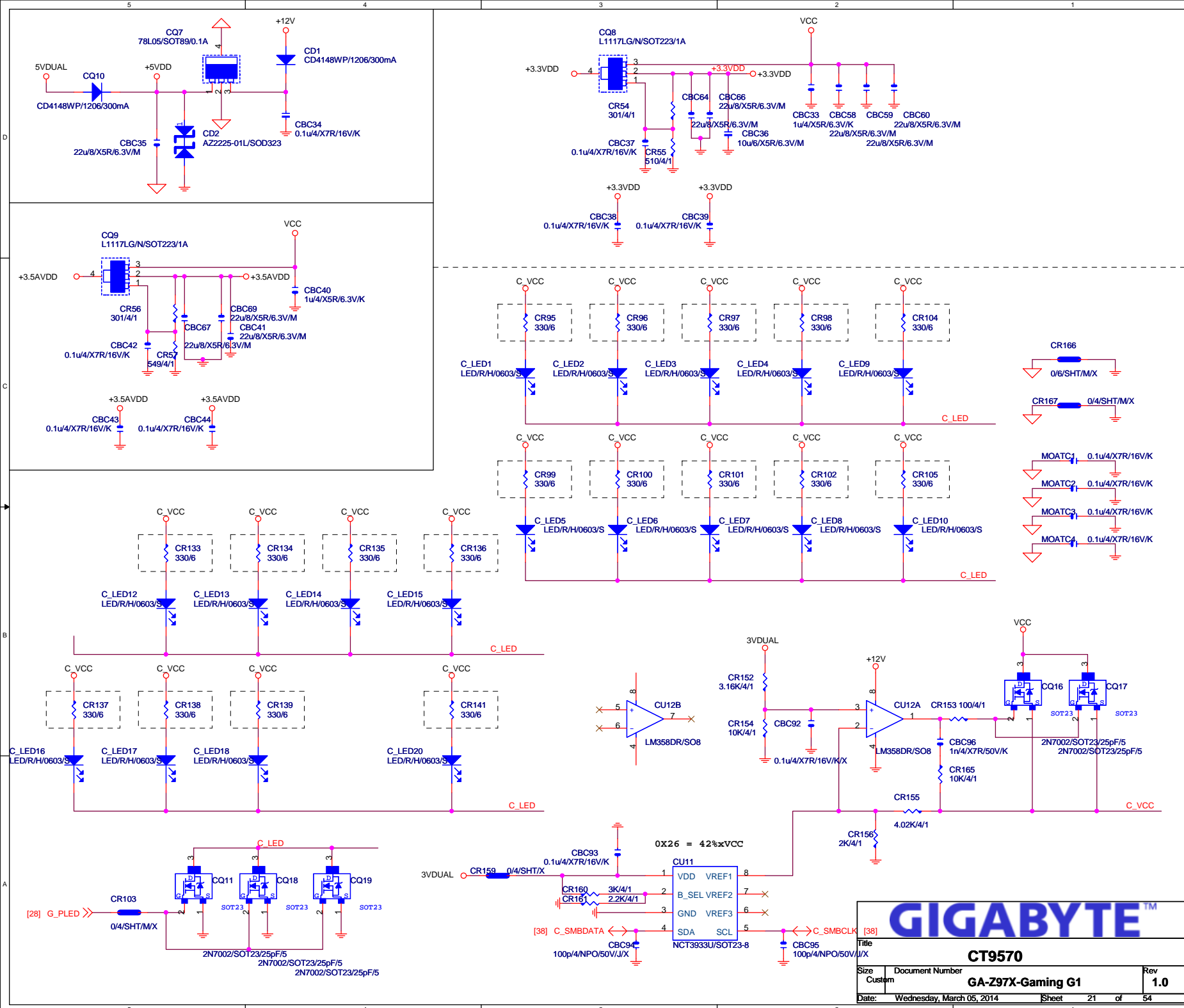


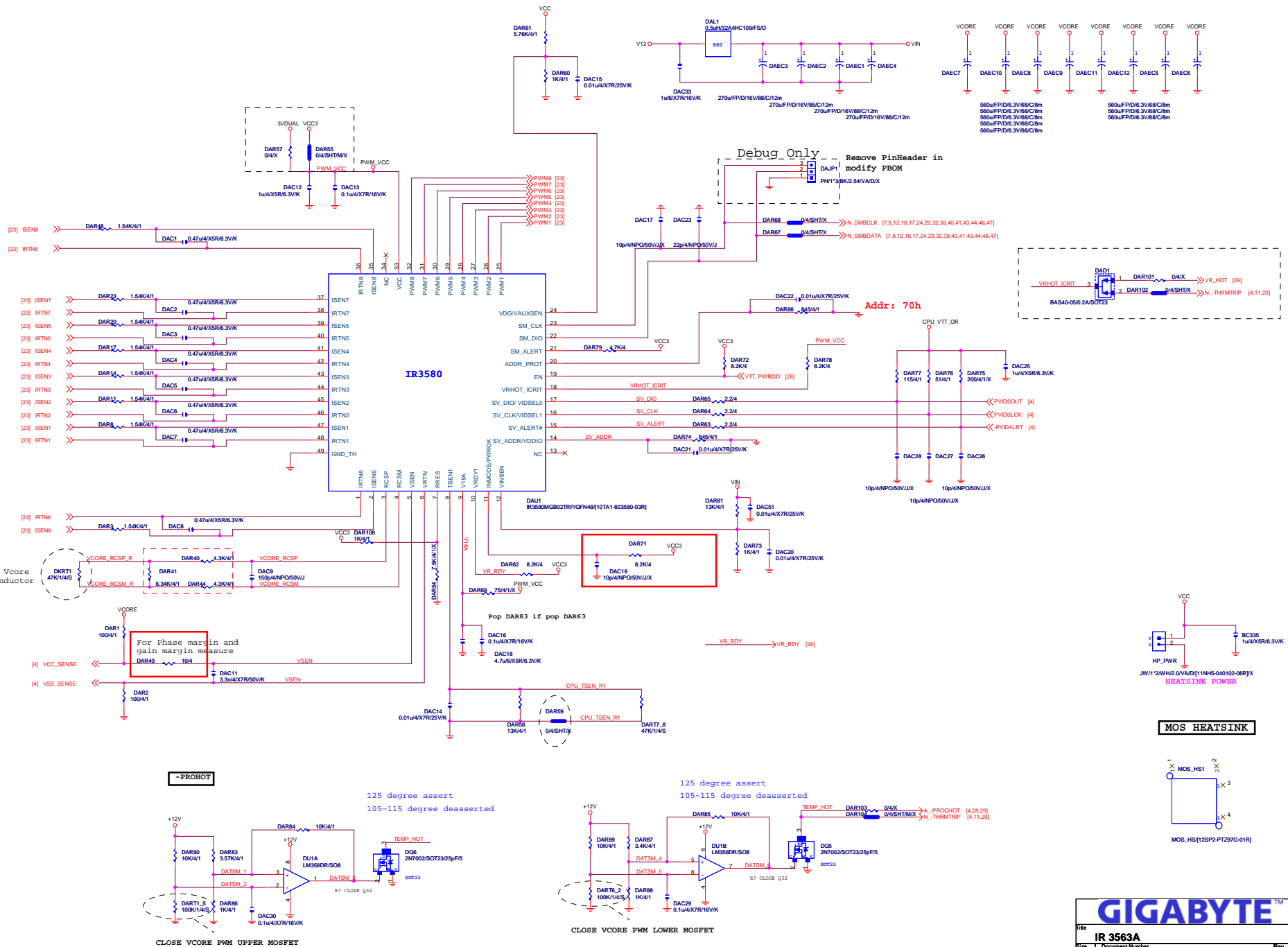
Rear SURROUND



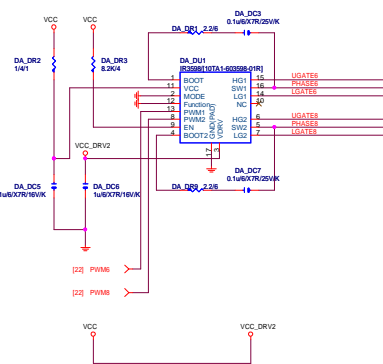
HD Audio FRONT PANEL







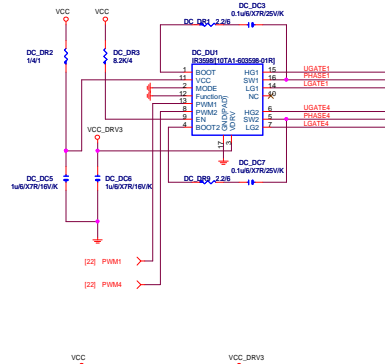
VCORE Phase 6,8



FUNCTION	MODE	PMN MODE	SWAGE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Seats	DUAL
1	0	Tri-Seats	Doubler
OPEN	0	Tri-Seats	Quad
close	1	Tri-Seats	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without SW

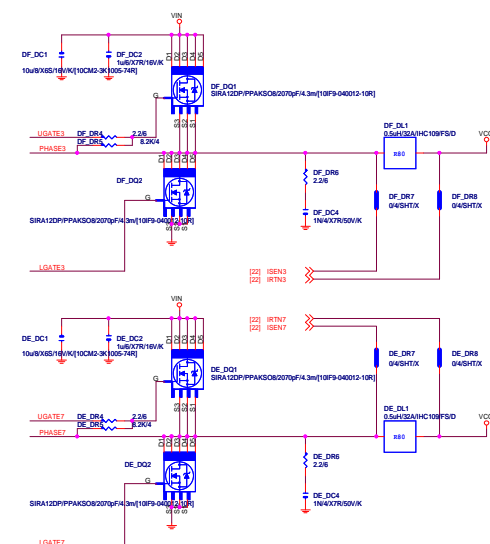
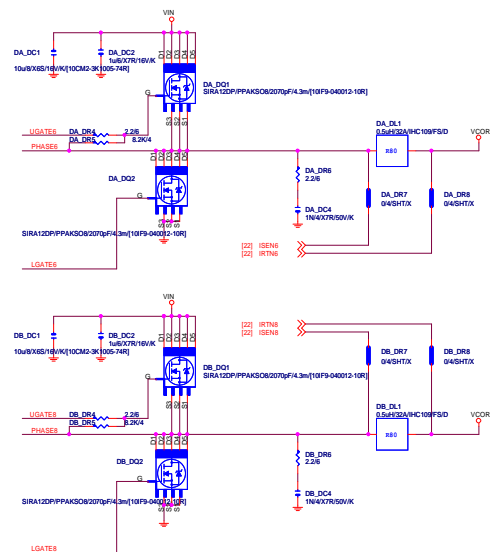
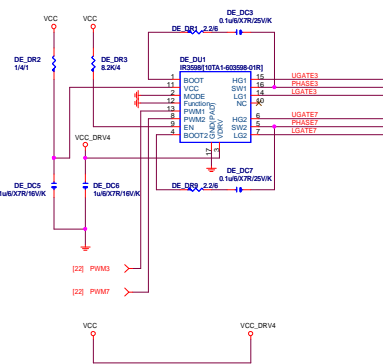
VCORE Phase 1,4



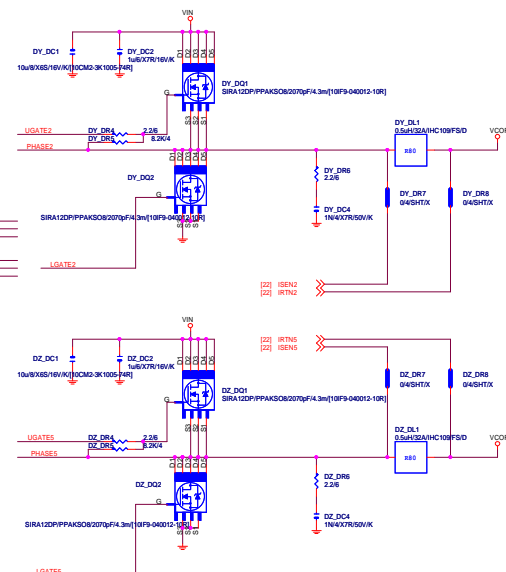
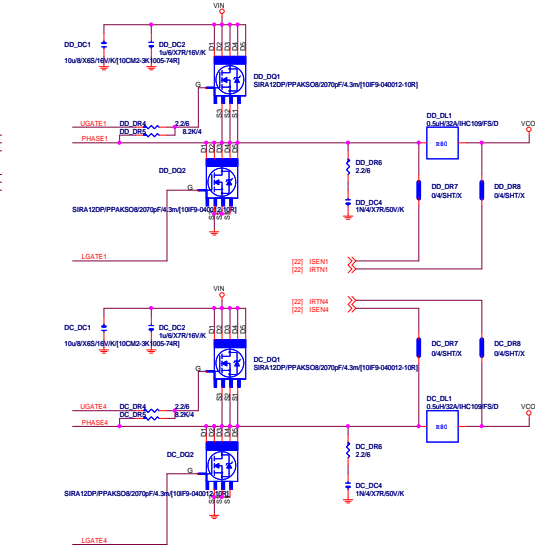
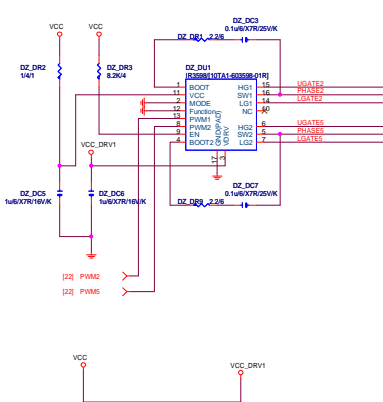
FUNCTION	MODE	FSM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doublier
0	0	Tri-Steate	DUAL
1	0	Tri-Steate	Doublier
CPIN	0	Tri-Steate	Quad
CPIN	1	CPIN	CPIN

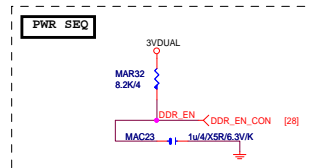
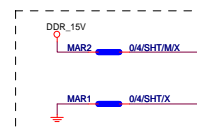
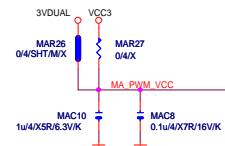
In Quad mode , IC1 pin10 link to IC2 pin10
and pin10 link to and pin10 link to

VCORE Phase 3,7

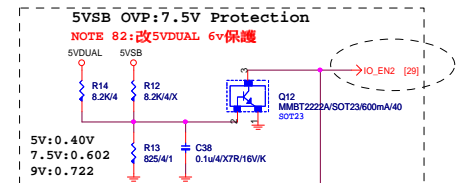
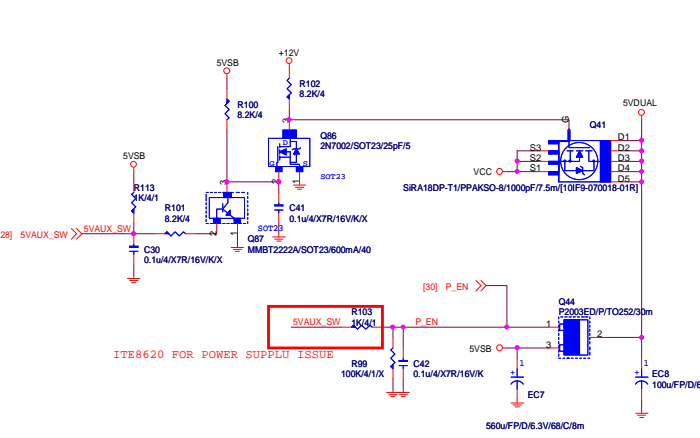


VCORE Phase 2,5

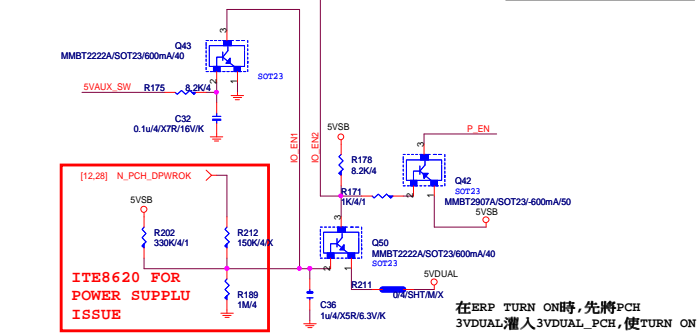




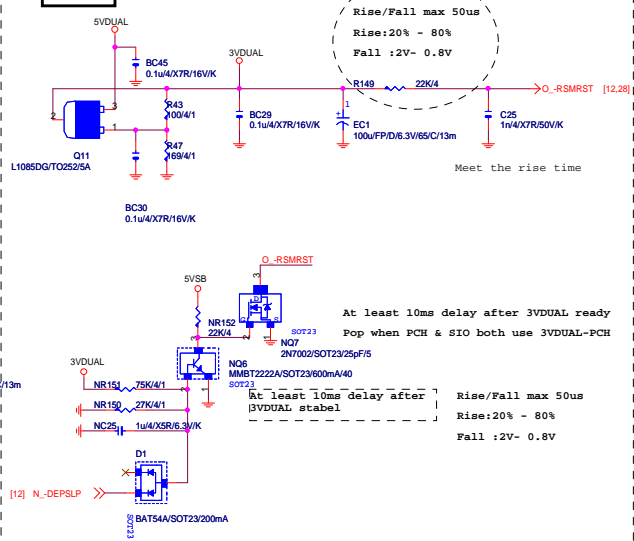
5VDUAL



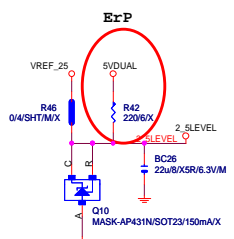
5VDUAL SHORT PROTECT



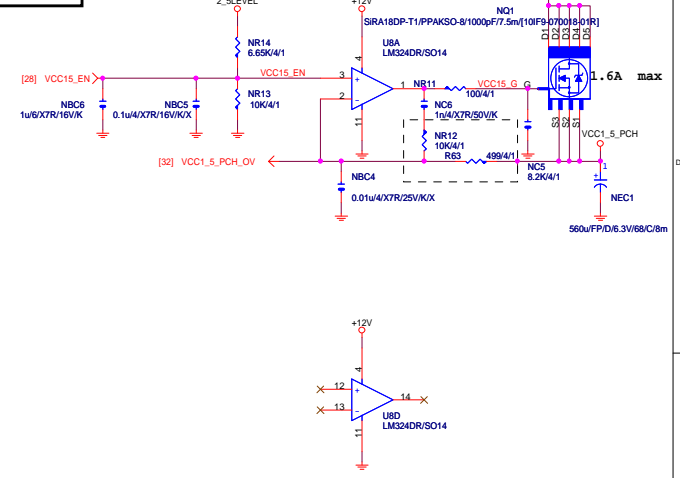
3VDUAL

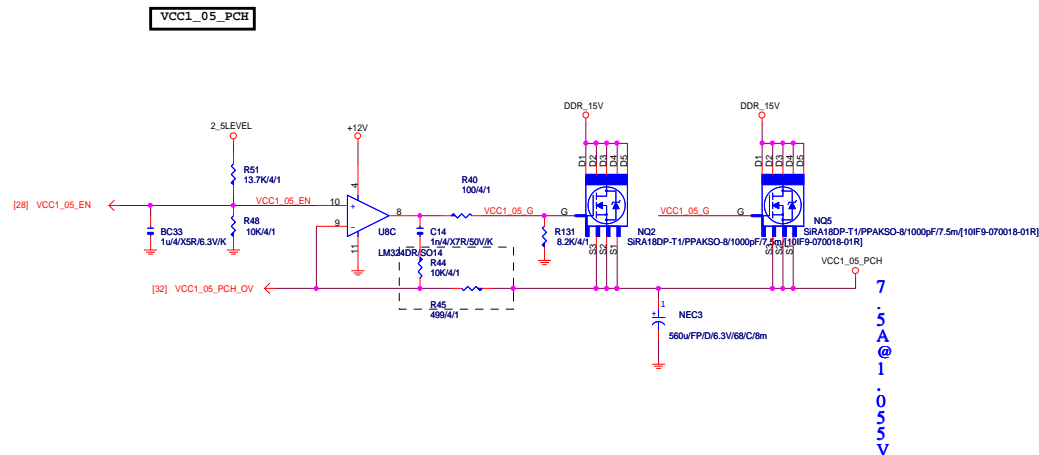


2_5LEVEL

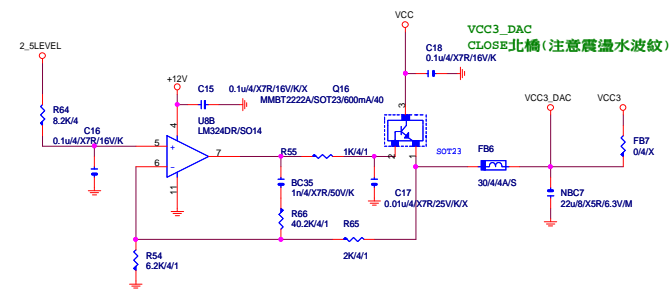


VCC1_5_PCH



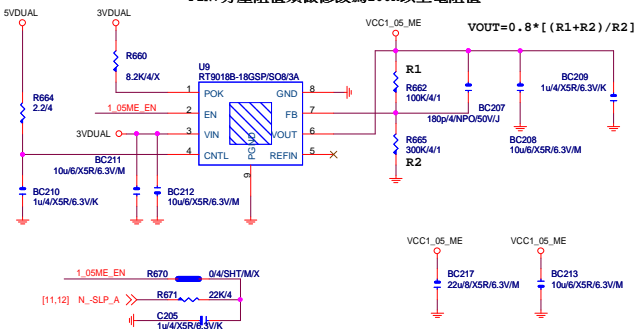


VCC3_DAC
(3.3V/70mA+360uA)

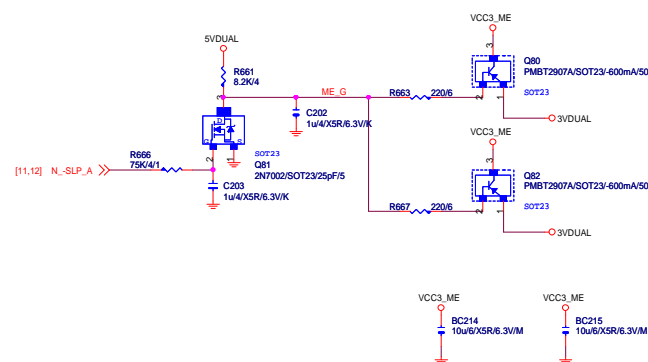


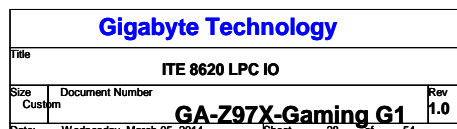
VCC1_05_ME

【技術通報R&D技術通報156】
(RICHTER), (NUVOTON), (EMC) 做共用
PIN7分壓阻值須做修改為100K以上電阻值



VCC3_ME



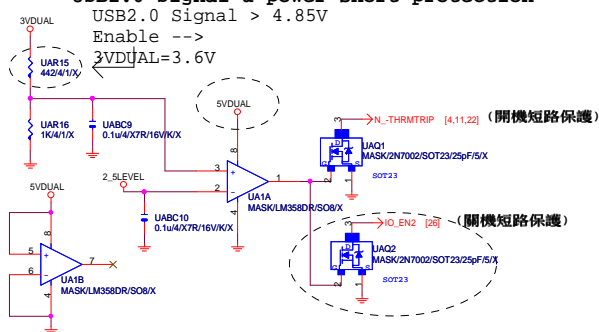


USB2.0 Signal & power short protection

USB2.0 Signal > 4.85V

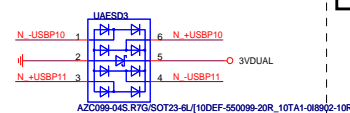
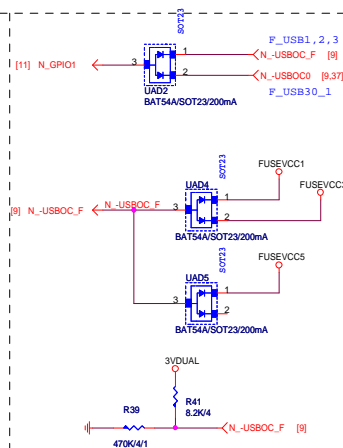
Enable -->

3VDUAL=3.6V

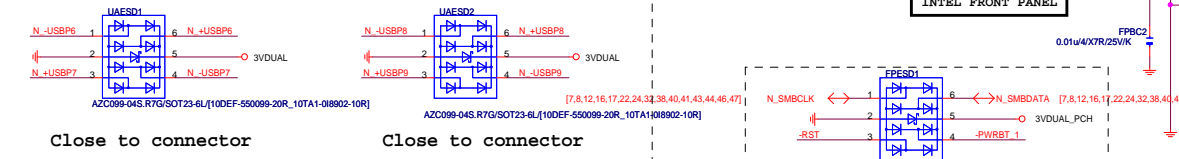
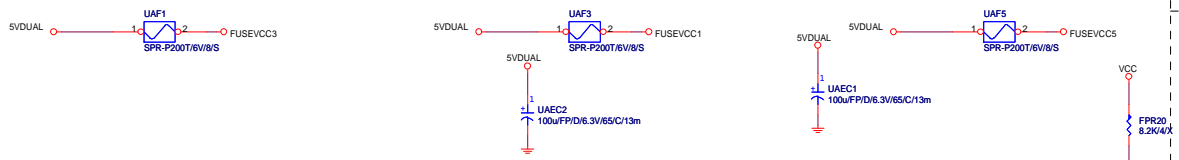
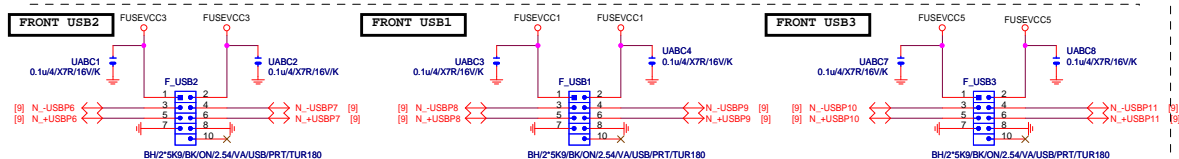


(開機短路保護)

(開機短路保護)

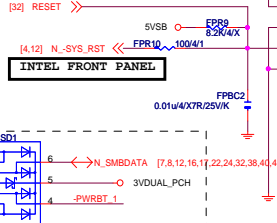


Close to connector

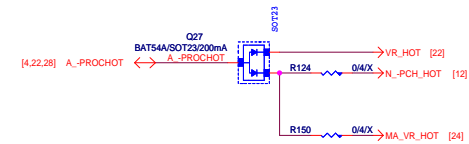


Close to connector

Close to connector



先進ESD再進PCH

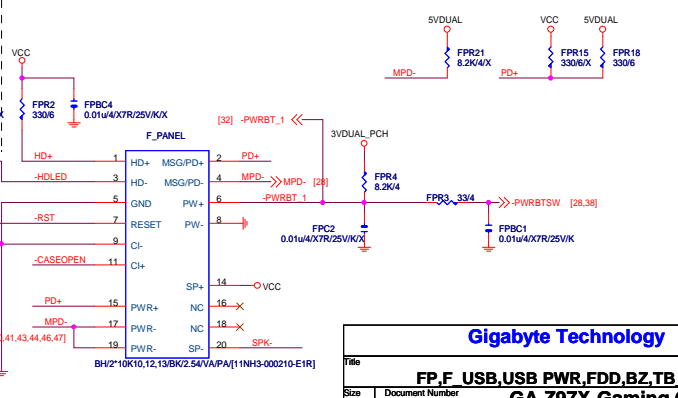
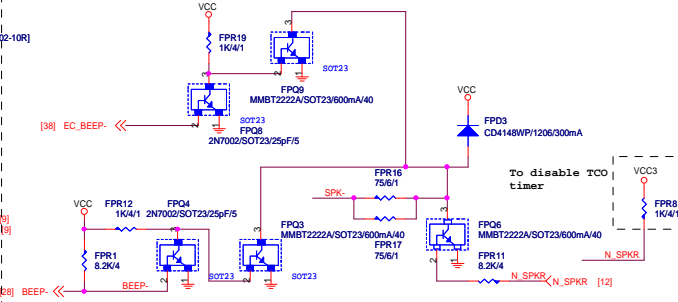


CASE OPEN

SATA LED

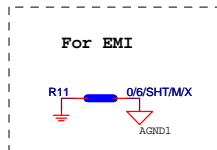
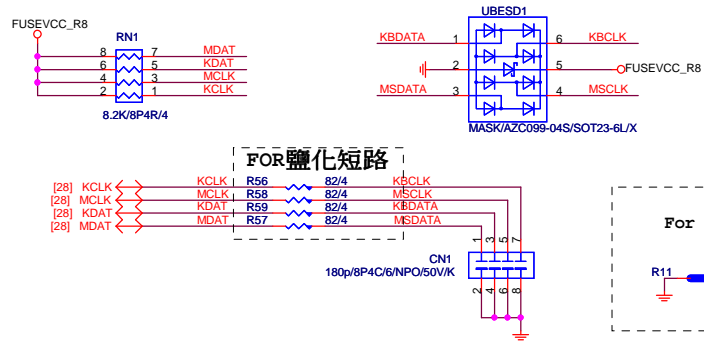
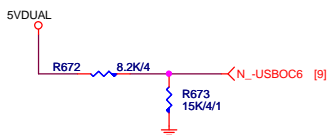
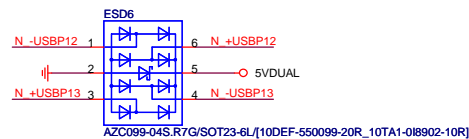
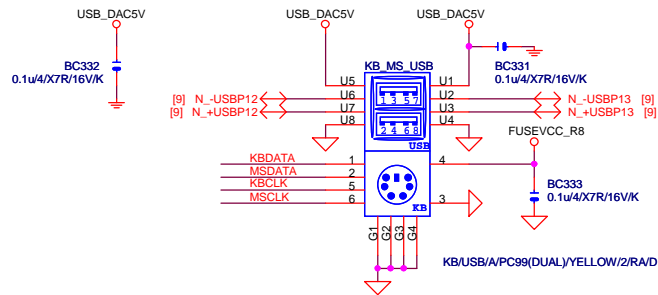
SATA LED

SPEAKER

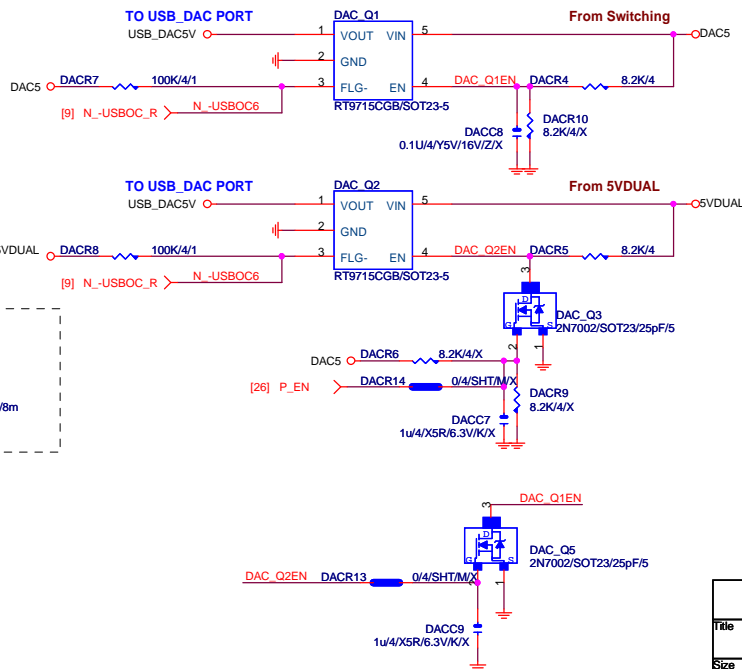
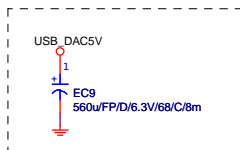
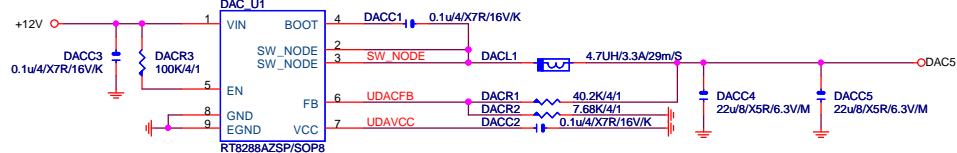


Gigabyte Technology

Title		FP.F_USB,USB PWR,FDD,BZ,TB_C
Size	Document Number	GA-Z97X-Gaming G1
Date	Wednesday, March 05, 2014	Sheet 29 of 54

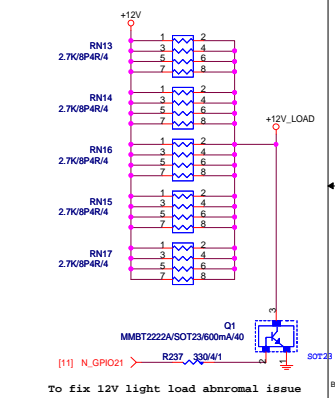
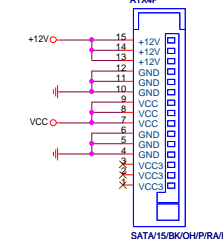
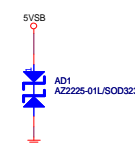
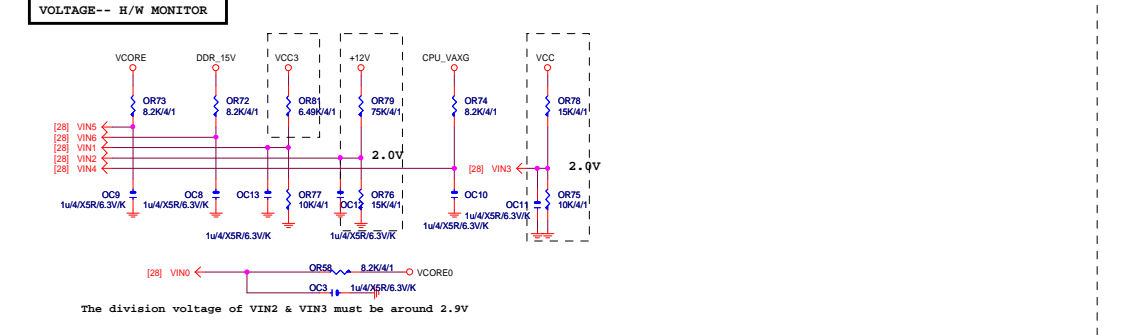
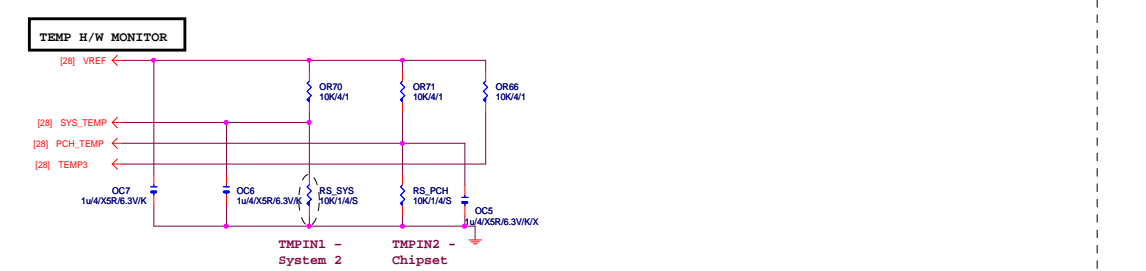
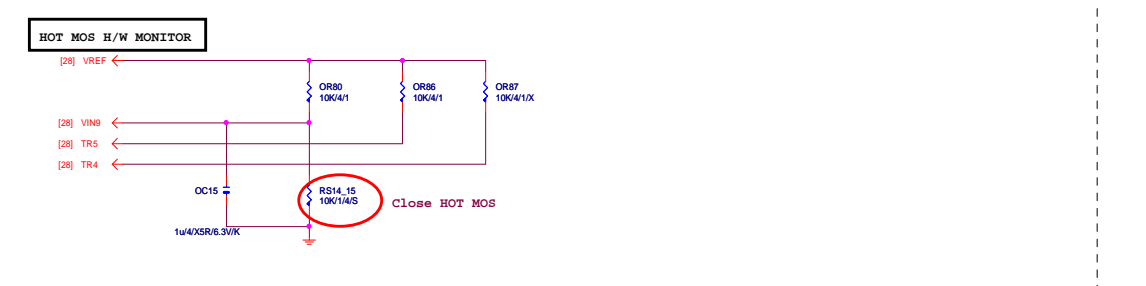
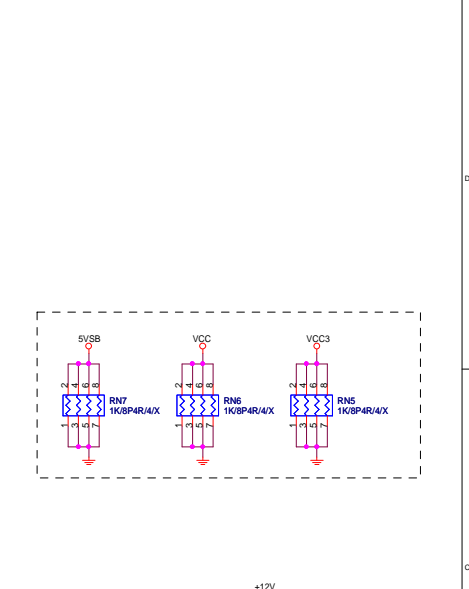
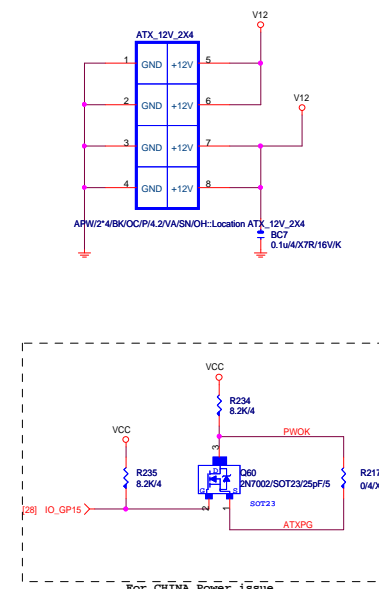
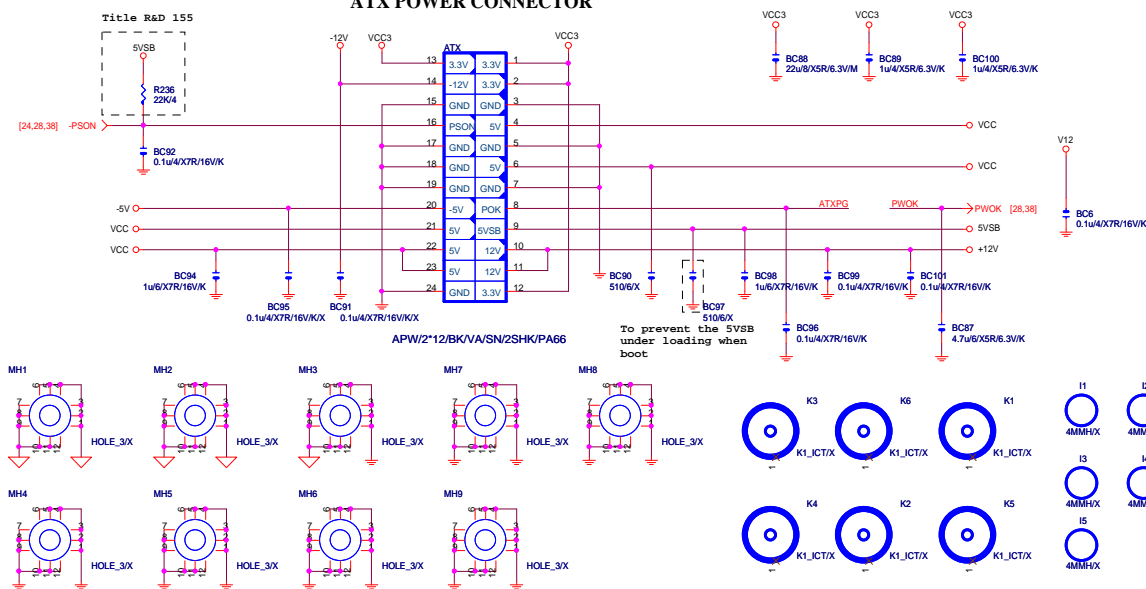


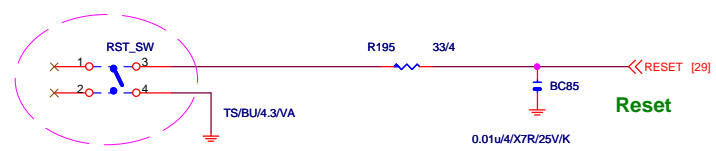
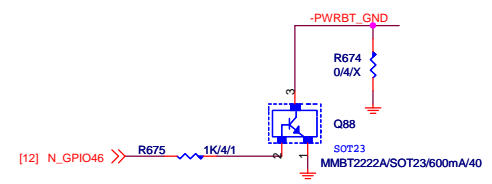
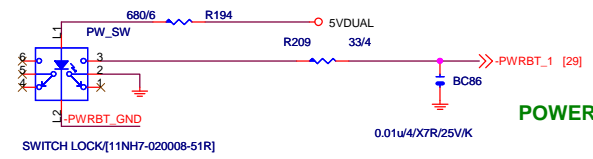
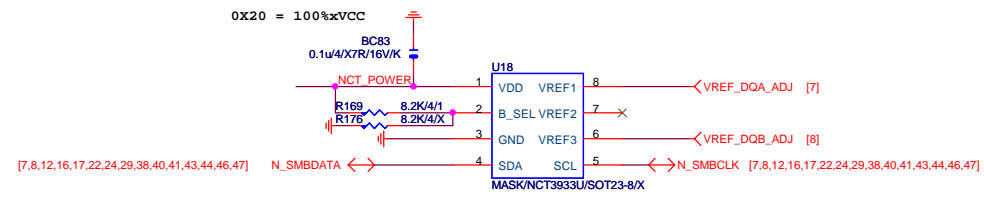
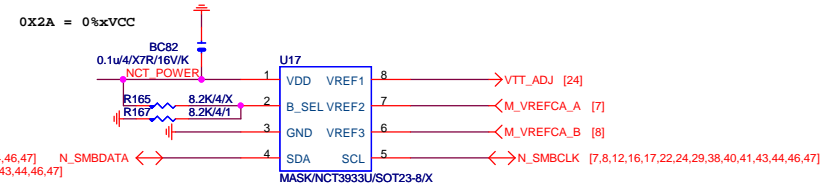
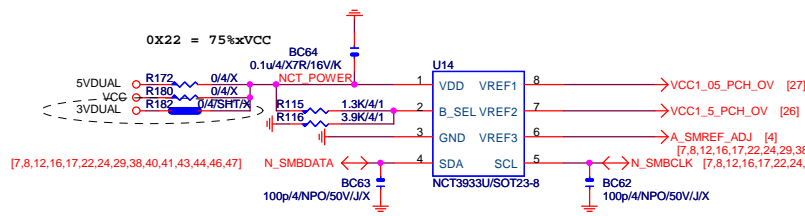
USB_DAC



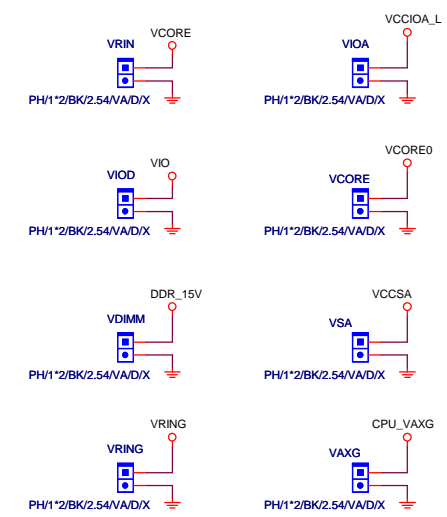
Gigabyte Technology			
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FP,F_USB,USB PWR,FDD,BZ			
Size			
Document Number			
GA-Z97X-Gaming G1.0			
Date: Wednesday, March 05, 2014			
Sheet 30 of 54			

ATX POWER CONNECTOR

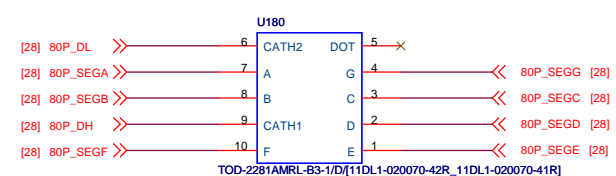
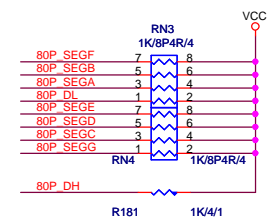




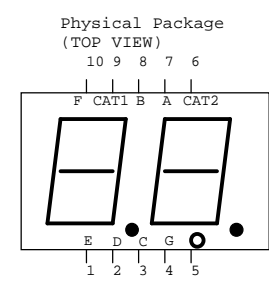
Clear CMOS



80 PORT



COMMON CATHODE



GIGABYTE™

Title: RST, PWR, CLR_CMOS

Size: Document Number

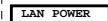
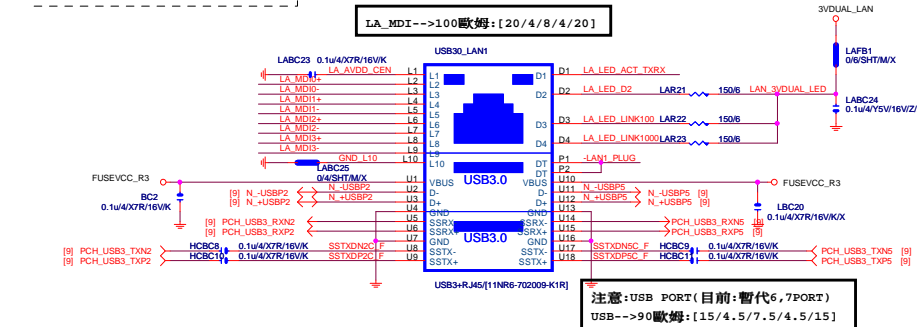
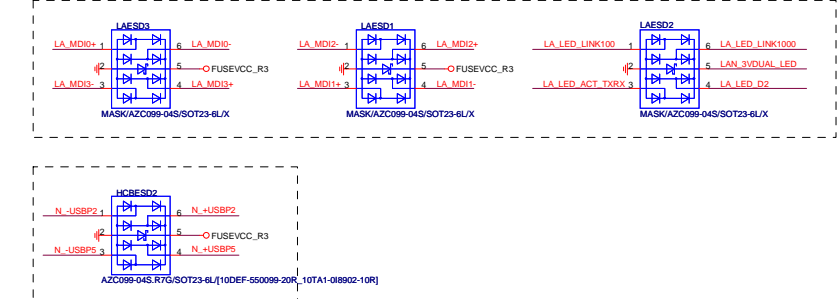
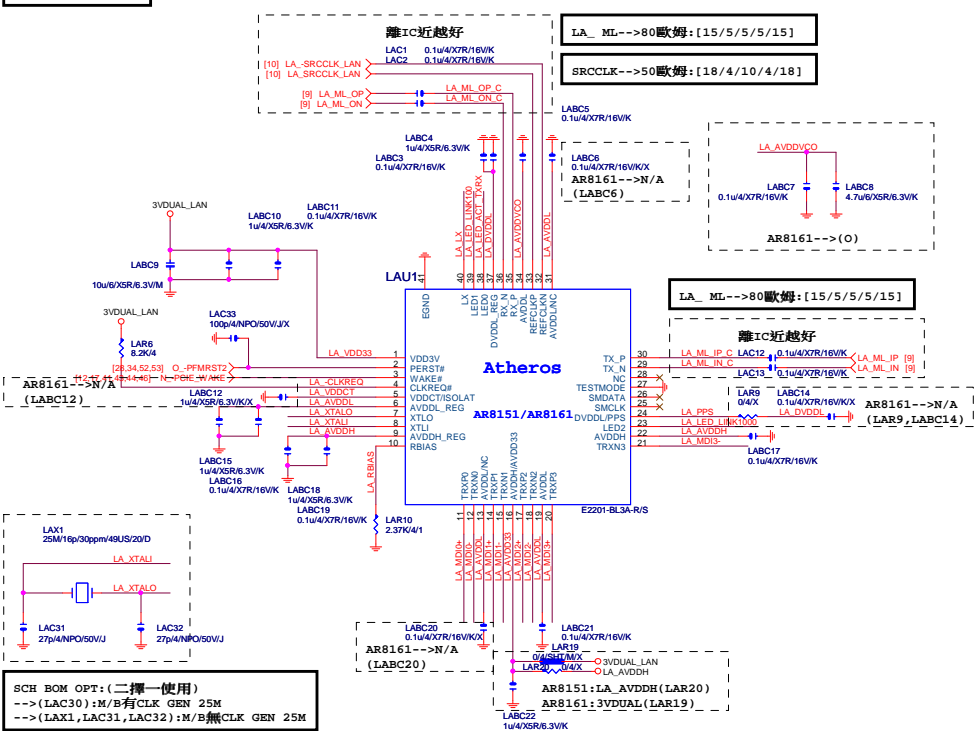
Custom: GA-Z97X-Gaming G1

Date: Wednesday, March 05, 2014

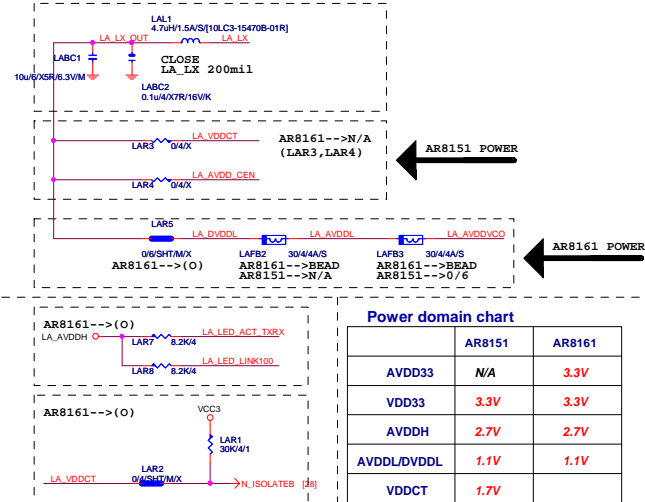
Sheet: 32 of 54

Rev: 1.0

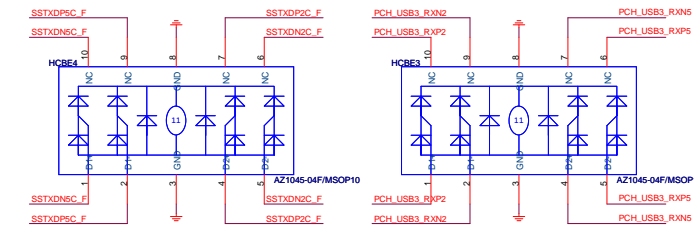
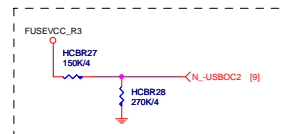
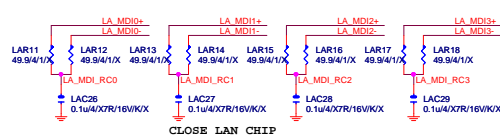
LAN:AR8151/AR8161



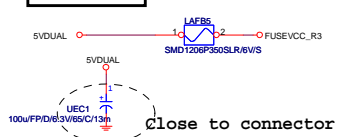
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NEW DESIGN ONLY FOR INTERNAL SWR
AR8151:LAR3(O),LAR5(X)
AR8161:LAR5(O),LAR3/LAR4(X)
```

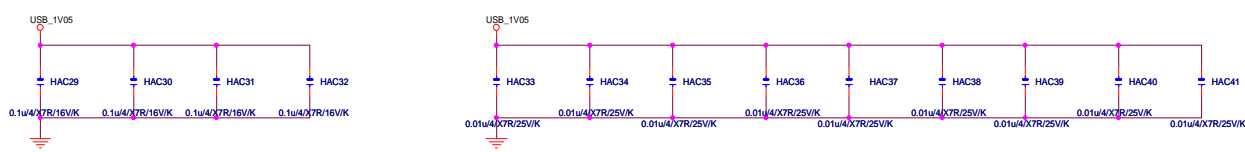
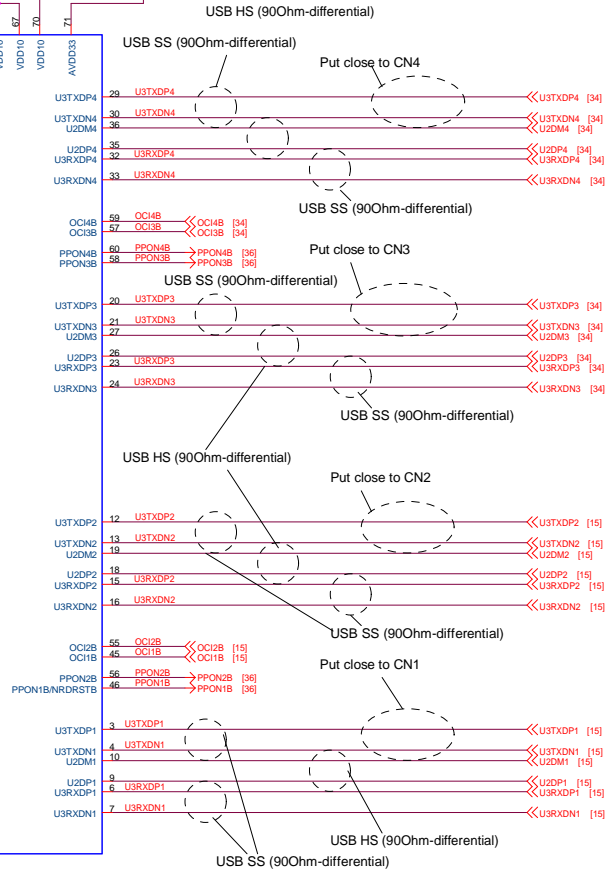
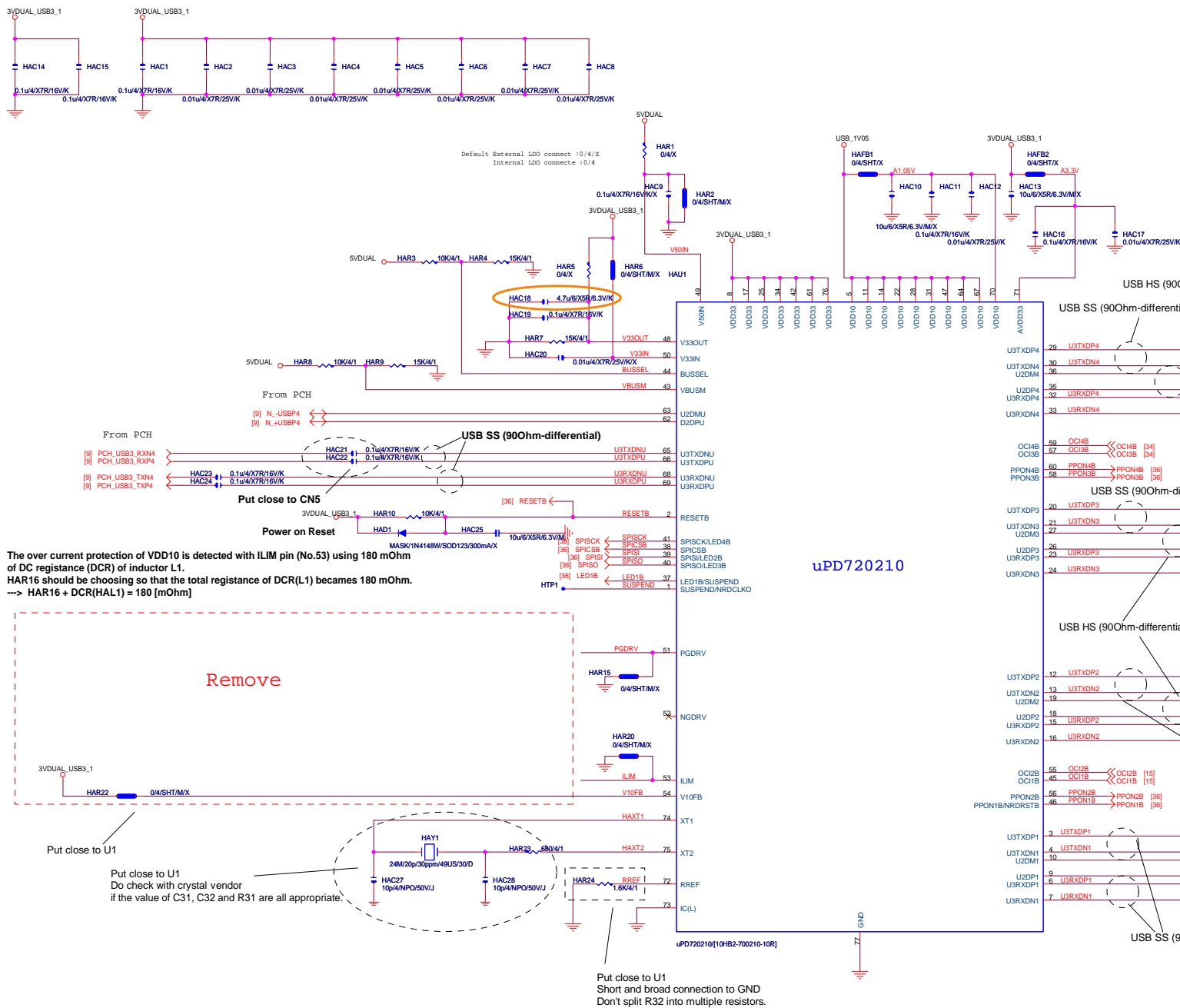


MDI : AR8161-->N/A

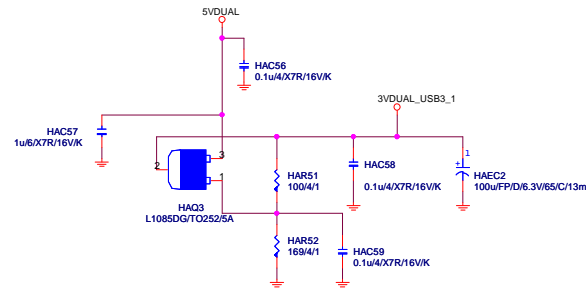


USB X3 POWER

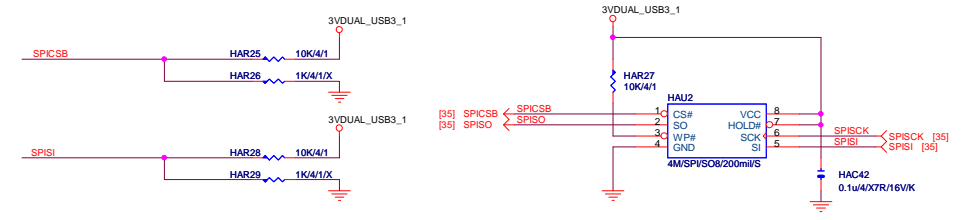




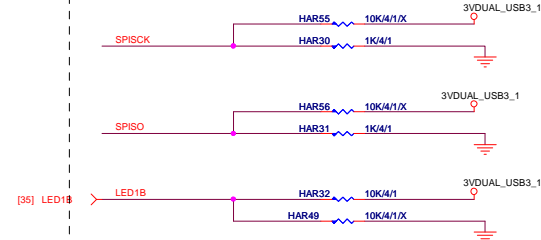
3VDUAL_USB



External SPI ROM ; SPI ROM attached mode

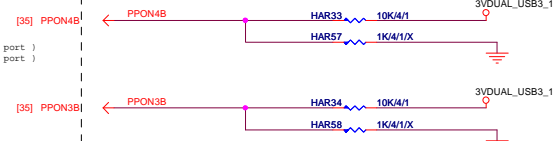


Battery Charging



Number of Ports ; 4Ports mode

PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)



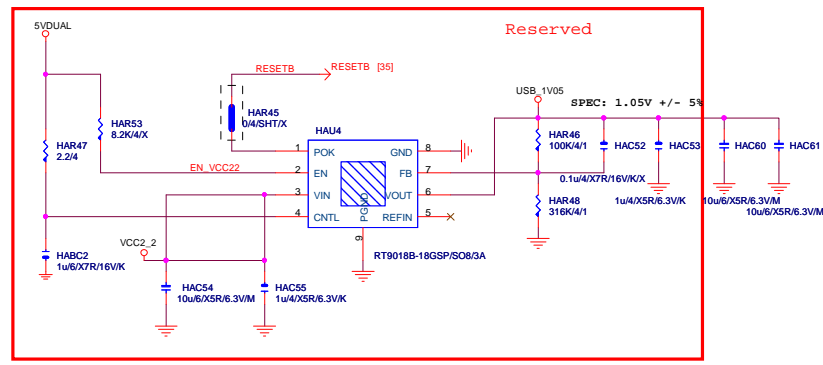
VBUS Power Control ; Individual mode

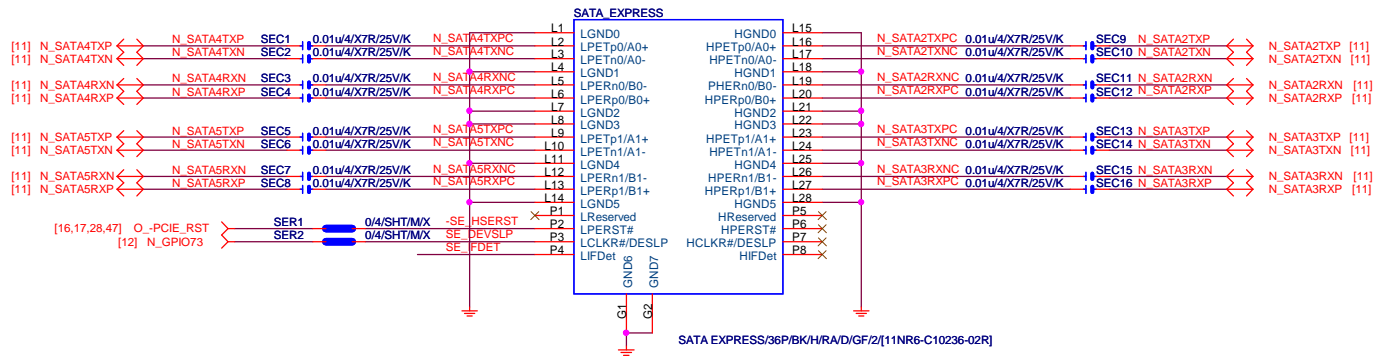
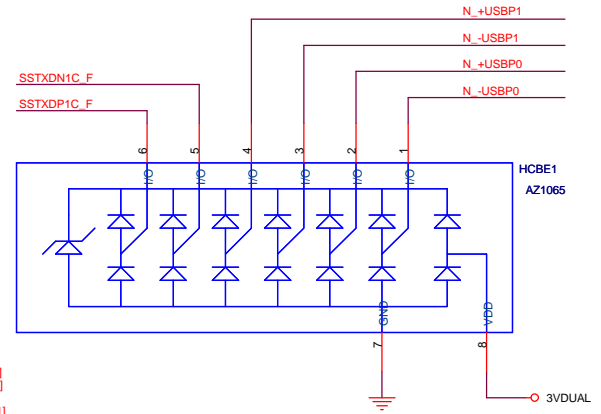
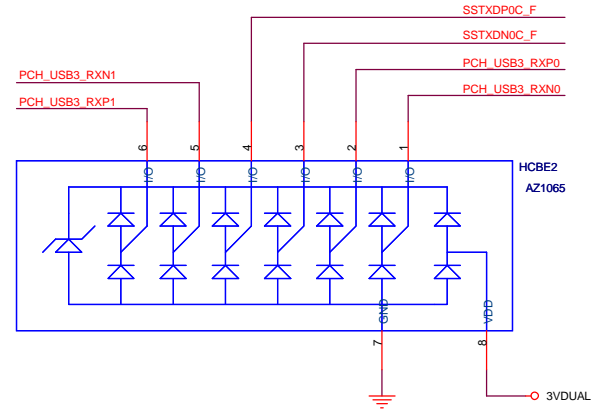
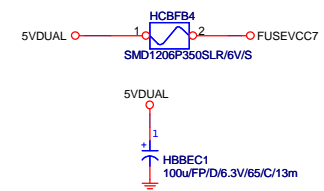
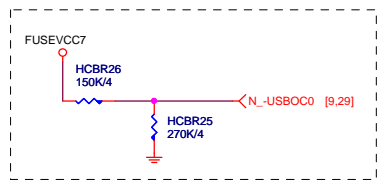
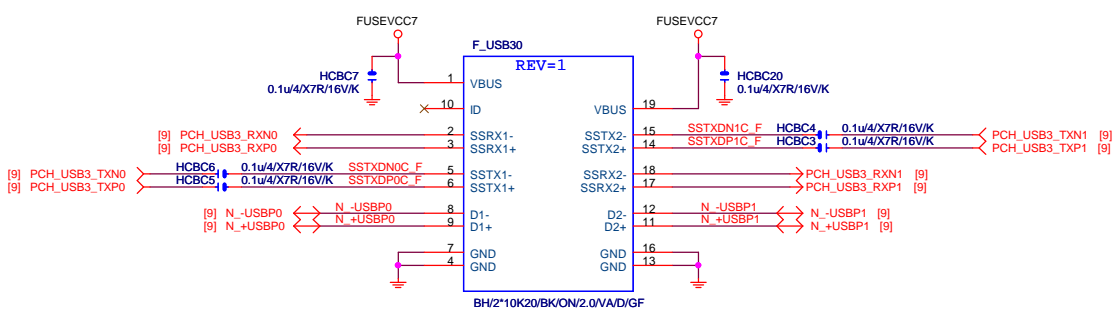


PPON1B Pin Function ; Port1 PPONB mode

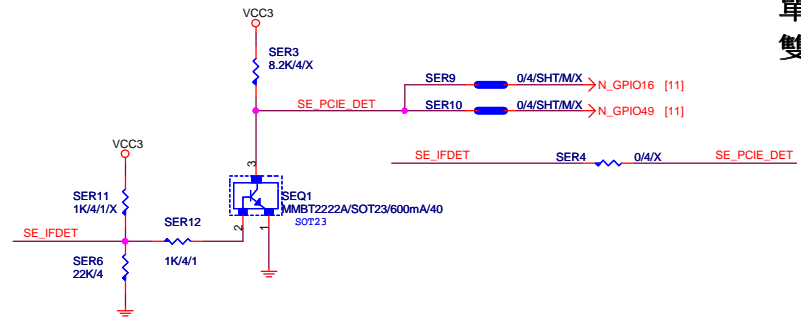


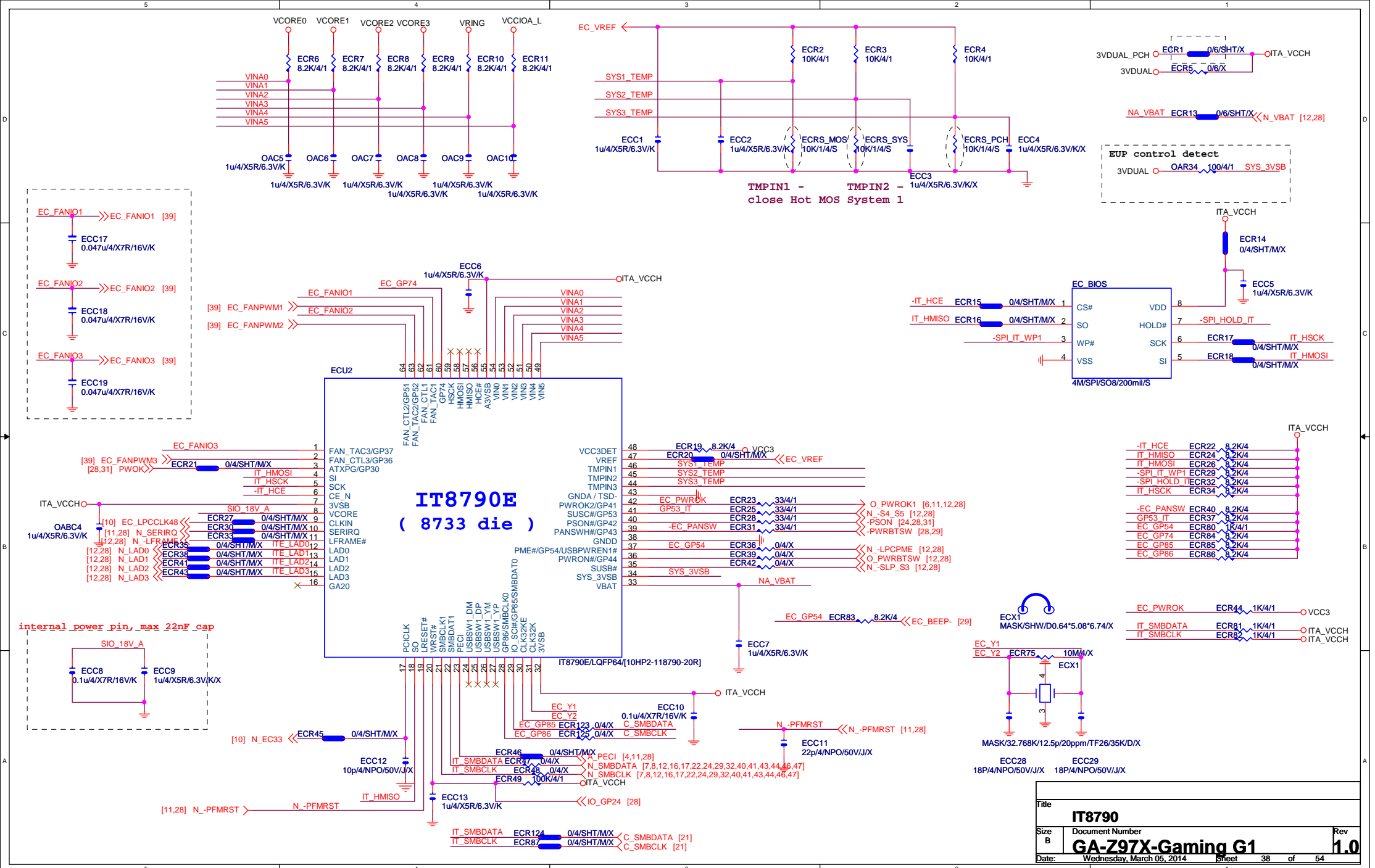
Reserved



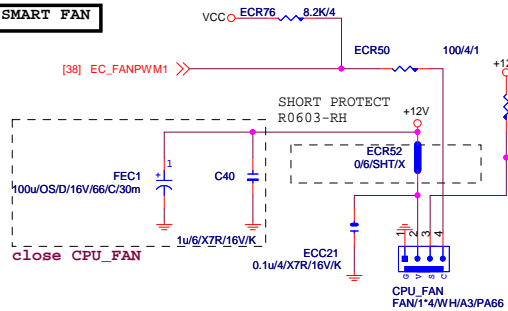


SATA EXPRESS料號
單層:11NR6-C10118-01R
雙層:11NR6-C10236-01R

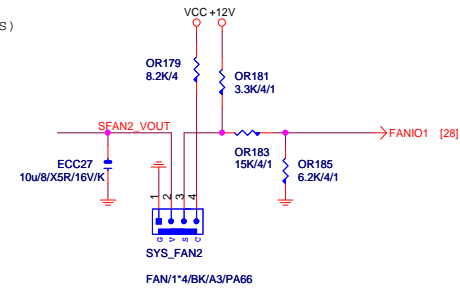
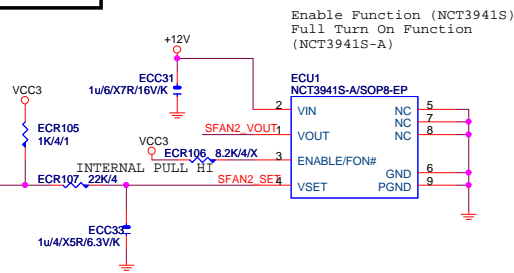




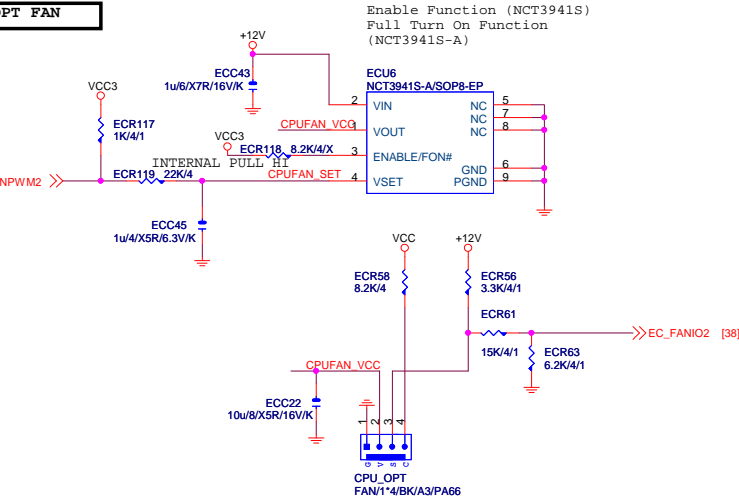
CPU SMART FAN



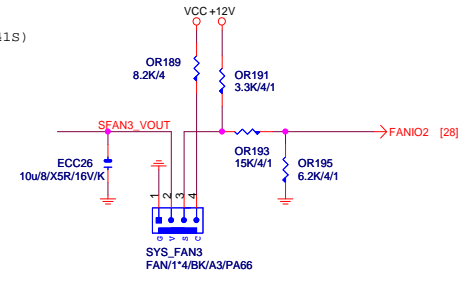
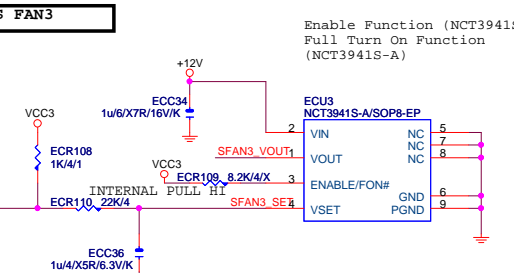
SYS FAN2



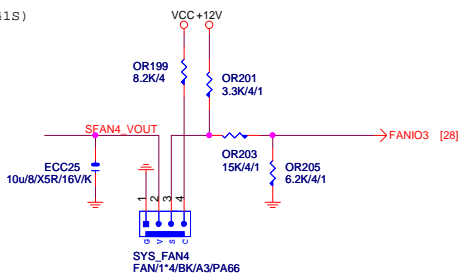
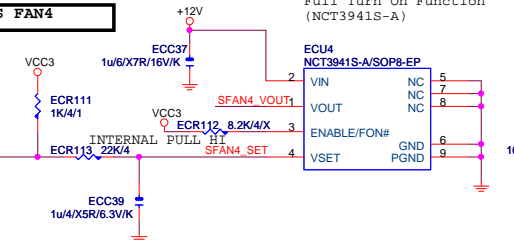
CPUOPT FAN



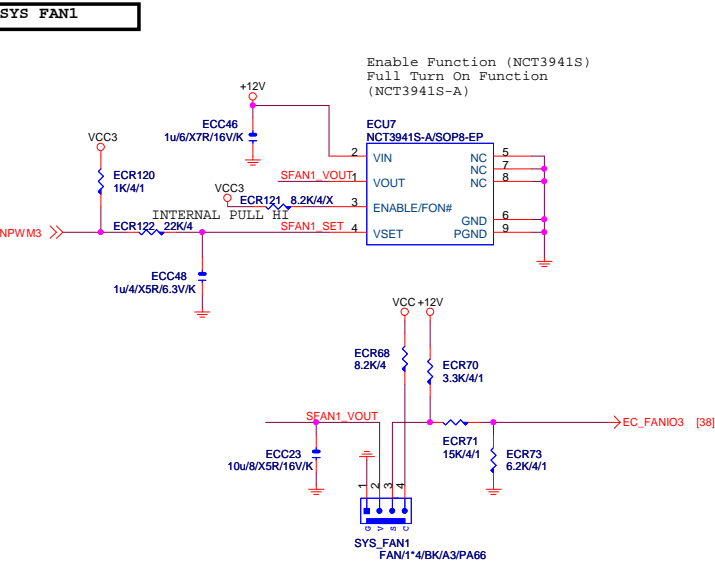
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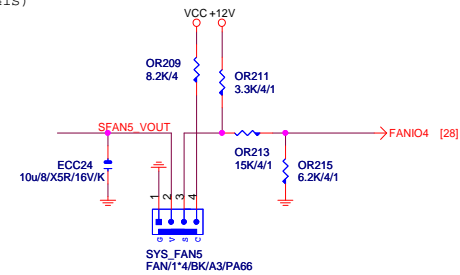
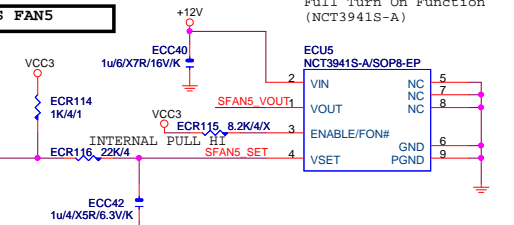
SYS FAN4



SYS FAN1

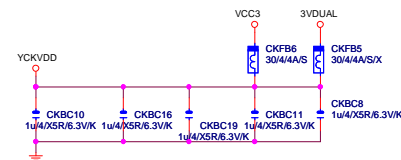
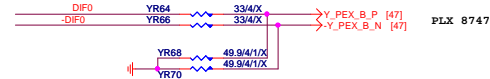
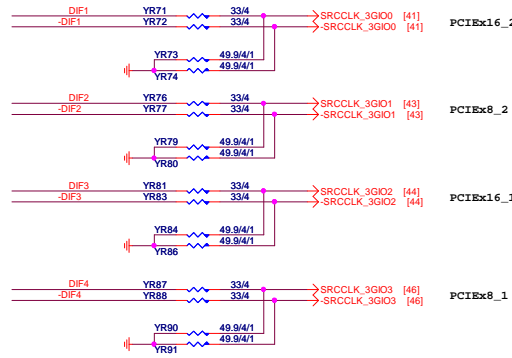
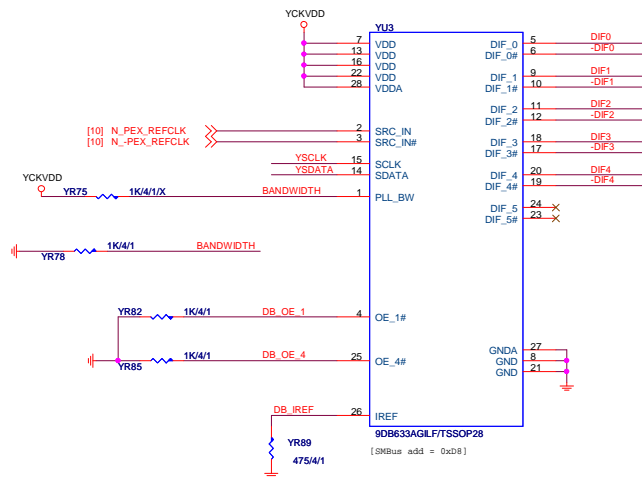


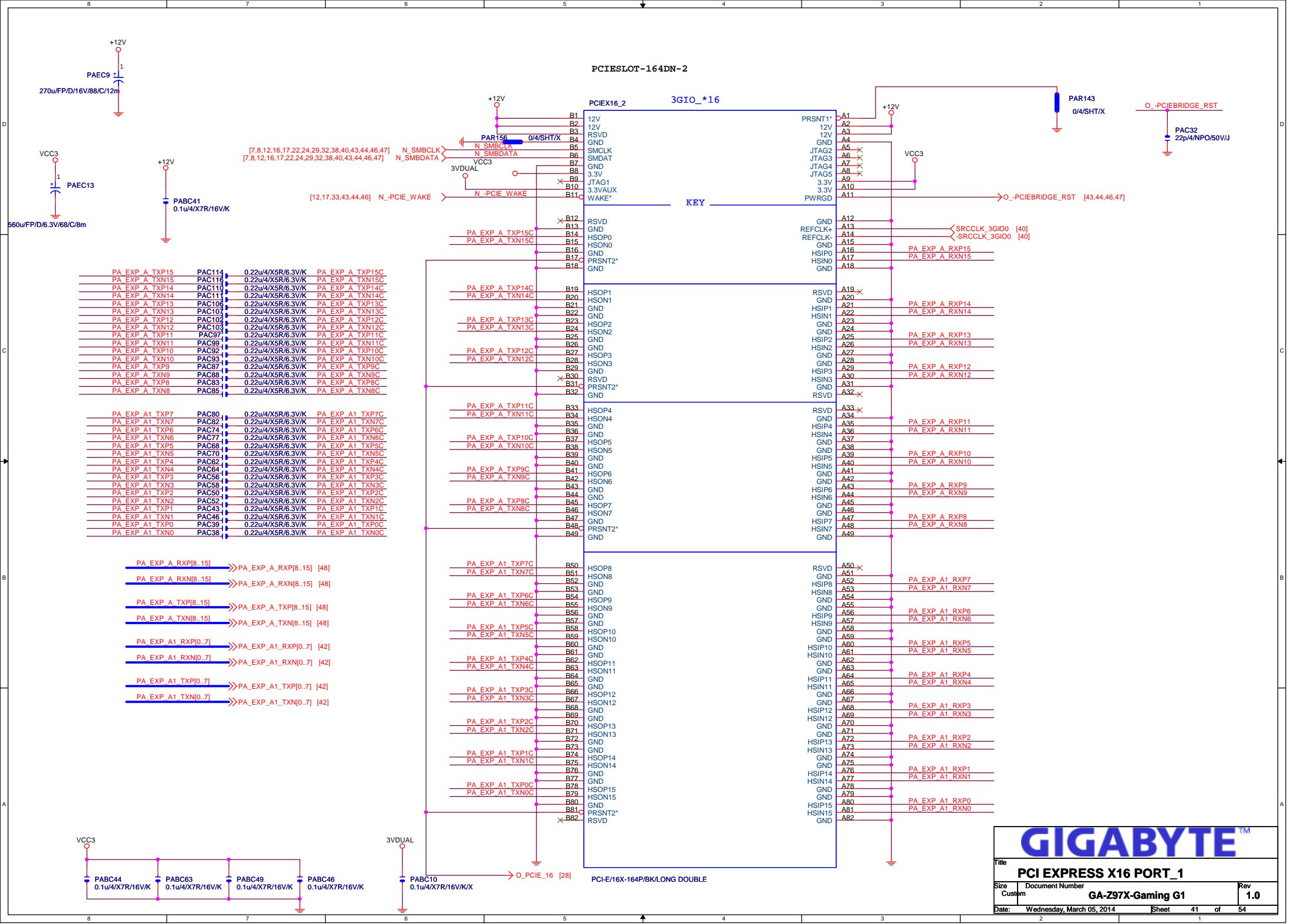
SYS FAN5

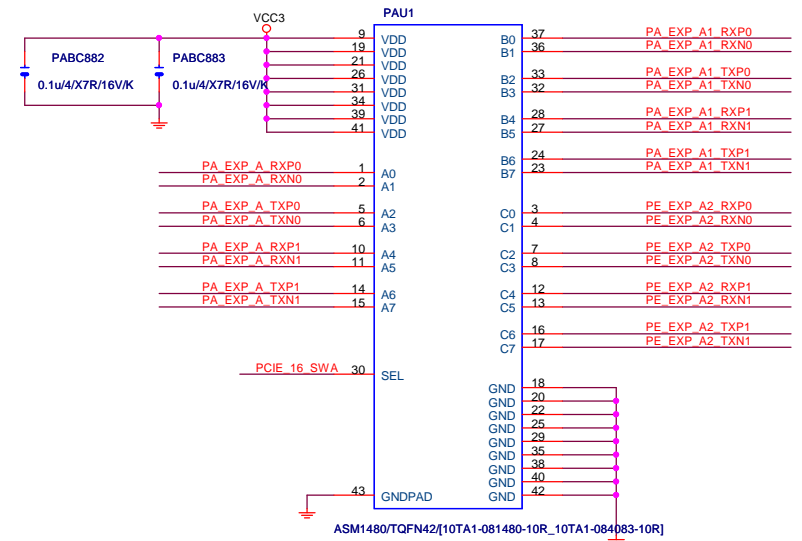
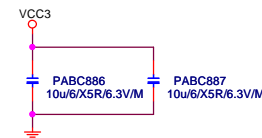
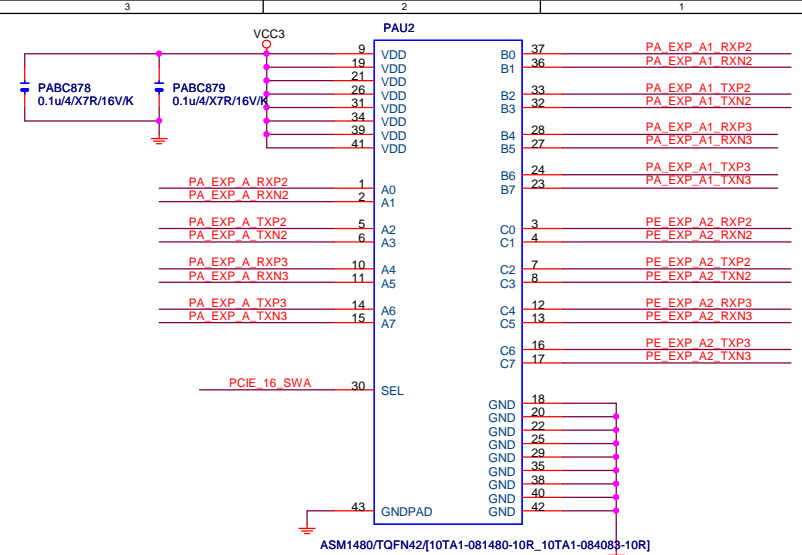


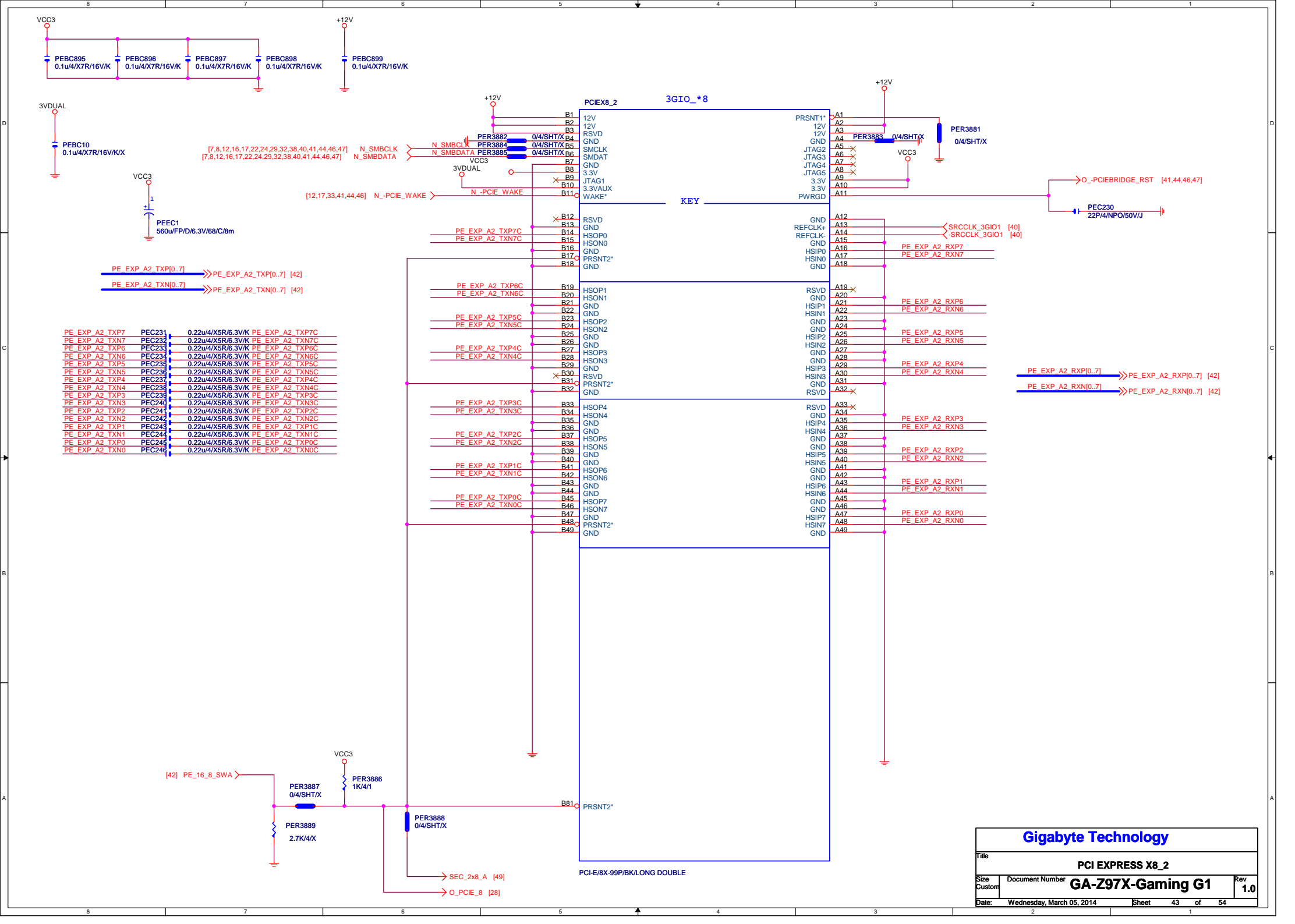
Gigabyte Technology

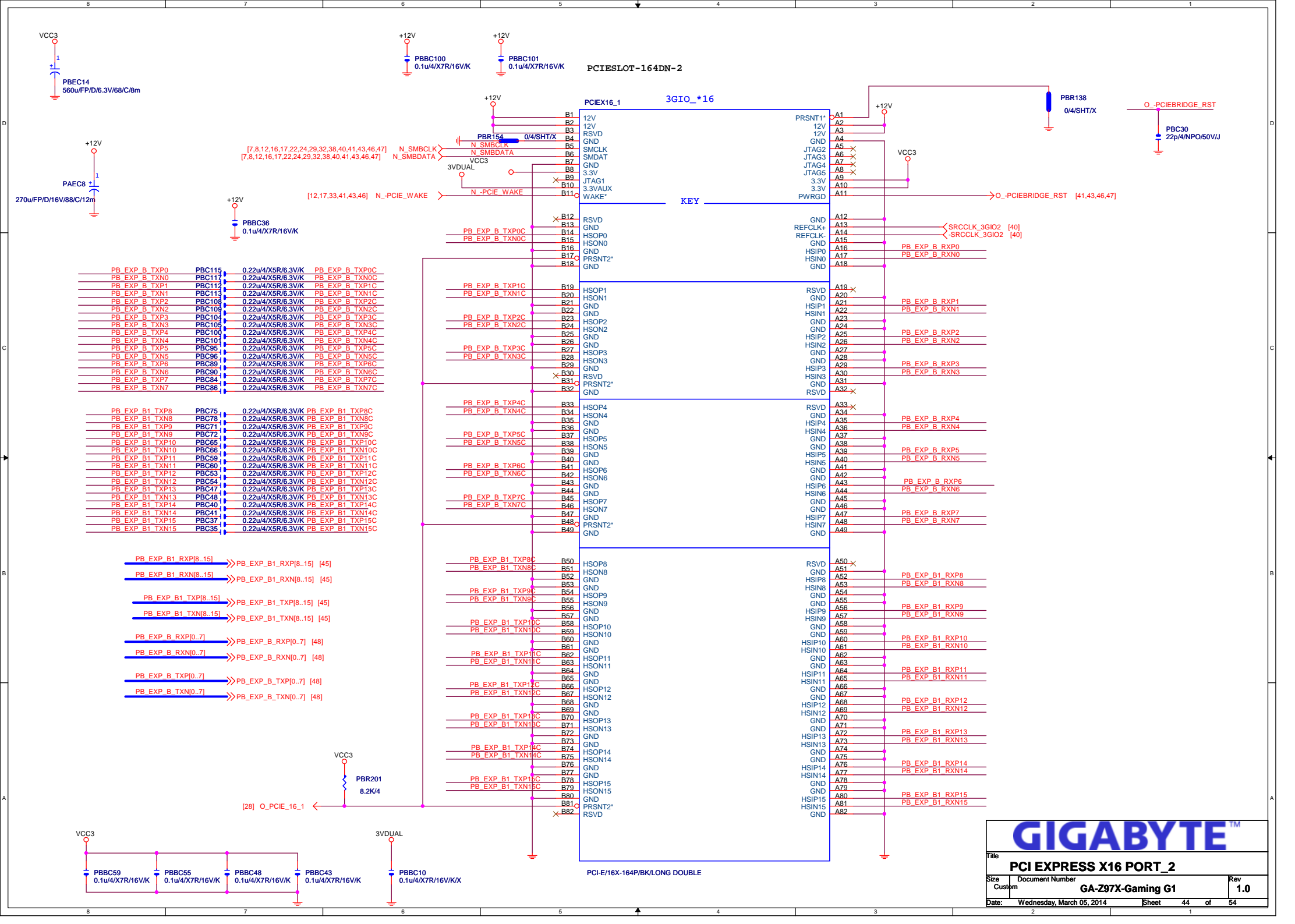
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Date:	Wednesday, March 05, 2014	Sheet 39 of 54

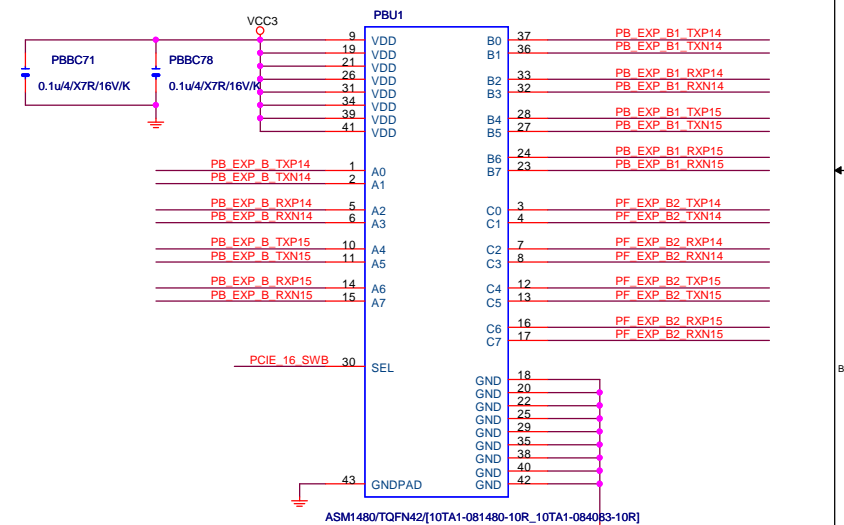
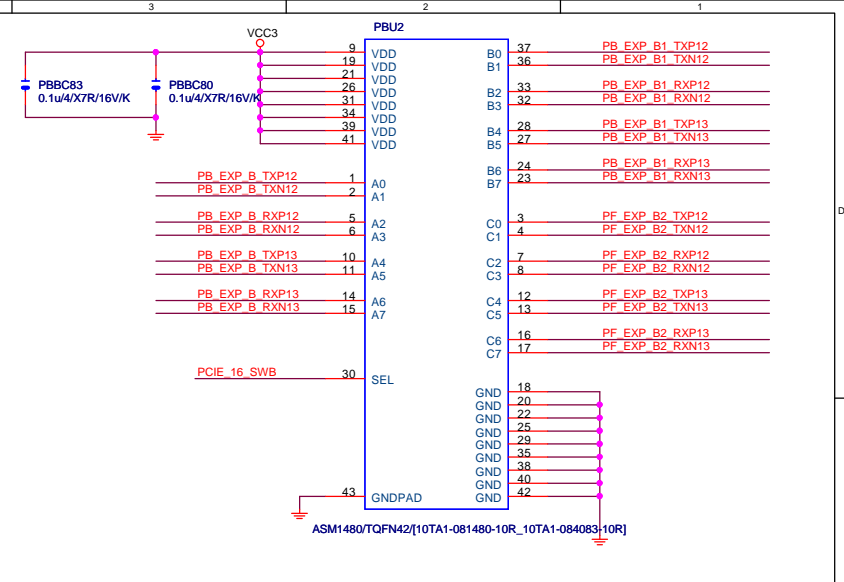


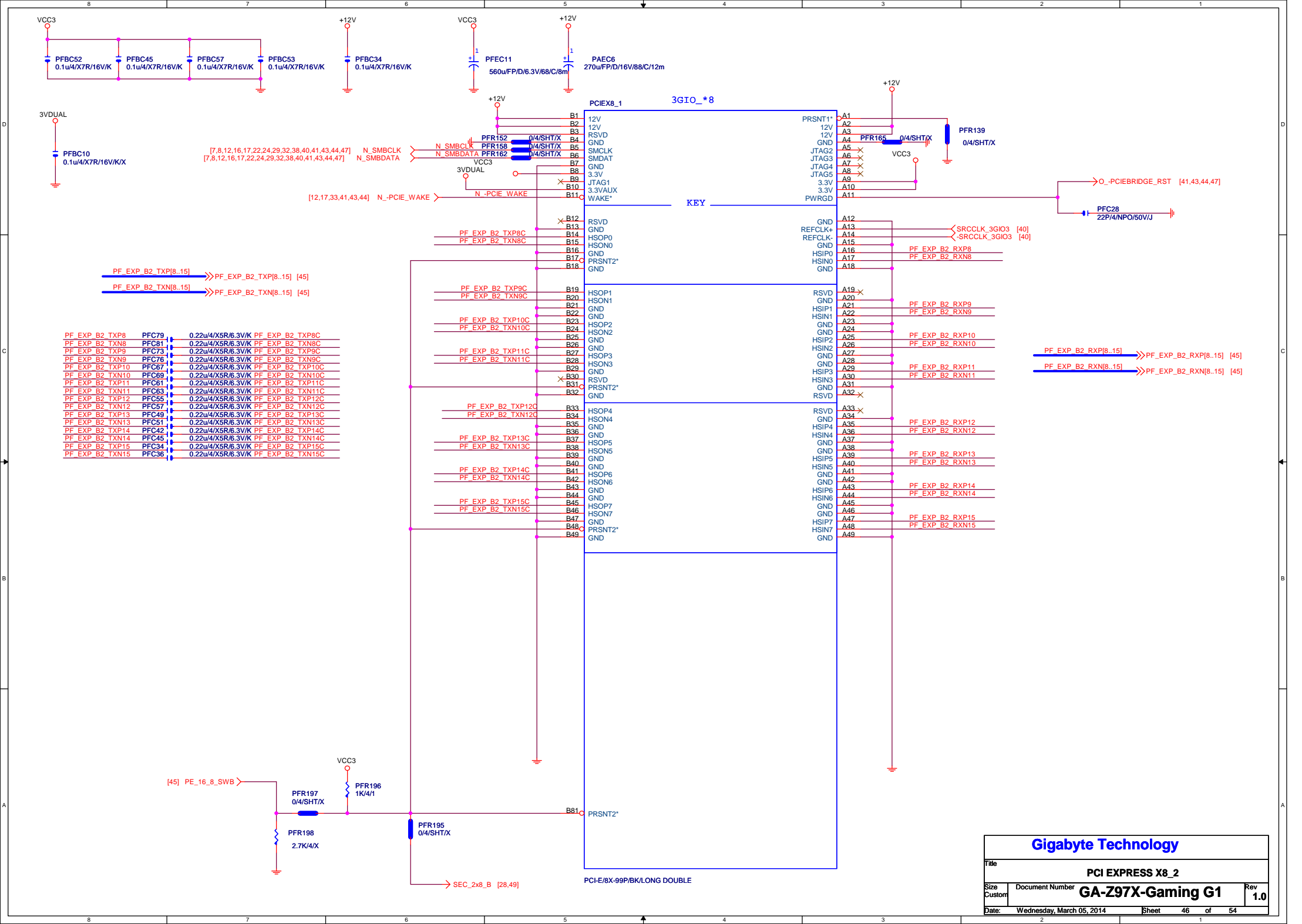












U18			
PA EXP A RXP0	V4	PEX_PERP16	V2
PA EXP A RXN0	V5	PEX_PERN16	V1
PA EXP A RXP1	U6	PEX_PERP17	U2
PA EXP A RXN1	U5	PEX_PERN17	U1
PA EXP A RXP2	R5	PEX_PERP18	R2
PA EXP A RXN2	R4	PEX_PERN18	R1
PA EXP A RXP3	P4	PEX_PERP19	P1
PA EXP A RXN3	M4	PEX_PERN19	M1
PA EXP A RXP4	L5	PEX_PERP20	L2
PA EXP A RXN4	L4	PEX_PERN20	L1
PA EXP A RXP5	J5	PEX_PERP21	J2
PA EXP A RXN5	J4	PEX_PERN21	J1
PA EXP A RXP6	H5	PEX_PERP22	H2
PA EXP A RXN6	H4	PEX_PERN22	H1
PA EXP A RXP7	E1	PEX_PERP23	E2
PA EXP A RXN7	E2	PEX_PERN23	E1
PA EXP A RXP8	D1	PEX_PERP24	D2
PA EXP A RXN8	D2	PEX_PERN24	D1
PA EXP A RXP9	C2	PEX_PERP25	C2
PA EXP A RXN9	C1	PEX_PERN25	C1
PA EXP A RXP10	B4	PEX_PERP26	B4
PA EXP A RXN10	B5	PEX_PERN26	B5
PA EXP A RXP11	A5	PEX_PERP27	A5
PA EXP A RXN11	A6	PEX_PERN27	A7
PA EXP A RXP12	D7	PEX_PERP28	D7
PA EXP A RXN12	D8	PEX_PERN28	D8
PA EXP A RXP13	E10	PEX_PERP29	E10
PA EXP A RXN13	E11	PEX_PERN29	E11
PA EXP A RXP14	D10	PEX_PERP30	D10
PA EXP A RXN14	D11	PEX_PERN30	D11
PA EXP A RXP15	E11	PEX_PERP31	E11
PA EXP A RXN15	D11	PEX_PERN31	A11
PB EXP B RXP0	V19	PEX_PERP32	V22
PB EXP B RXN0	V20	PEX_PERN32	V23
PB EXP B RXP1	U19	PEX_PERP33	U22
PB EXP B RXN1	U20	PEX_PERN33	U23
PB EXP B RXP2	R19	PEX_PERP34	R22
PB EXP B RXN2	R20	PEX_PERN34	R23
PB EXP B RXP3	P19	PEX_PERP35	P22
PB EXP B RXN3	P20	PEX_PERN35	P23
PB EXP B RXP4	M19	PEX_PERP36	M22
PB EXP B RXN4	M20	PEX_PERN36	M23
PB EXP B RXP5	L19	PEX_PERP37	L22
PB EXP B RXN5	L20	PEX_PERN37	L23
PB EXP B RXP6	J19	PEX_PERP38	J22
PB EXP B RXN6	J20	PEX_PERN38	J23
PB EXP B RXP7	H19	PEX_PERP39	H22
PB EXP B RXN7	H20	PEX_PERN39	H23
PB EXP B RXP8	E23	PEX_PERP40	E23
PB EXP B RXN8	D23	PEX_PERN40	A23
PB EXP B RXP9	E22	PEX_PERP41	B22
PB EXP B RXN9	D22	PEX_PERN41	A22
PB EXP B RXP10	E20	PEX_PERP42	B20
PB EXP B RXN10	D20	PEX_PERN42	A20
PB EXP B RXP11	E19	PEX_PERP43	B19
PB EXP B RXN11	D19	PEX_PERN43	A19
PB EXP B RXP12	E17	PEX_PERP44	B17
PB EXP B RXN12	D17	PEX_PERN44	A17
PB EXP B RXP13	E16	PEX_PERP45	B16
PB EXP B RXN13	D16	PEX_PERN45	A16
PB EXP B RXP14	E14	PEX_PERP46	B14
PB EXP B RXN14	D14	PEX_PERN46	A14
PB EXP B RXP15	E13	PEX_PERP47	B13
PB EXP B RXN15	D13	PEX_PERN47	A13

SYSCLK_INP4 P7
 SYSCLK_INN4 P6

PEX_REFCLK_SSCP4
 PEX_REFCLK_SSCN4
 PEX_REFCLK_SSCP8
 PEX_REFCLK_SSCN8

P17 SYSCLK_INP8
 P18 SYSCLK_INN8

PEX8747BA0FBC08GA575

SYSCLK_INP4 YR17
 SYSCLK_INN4 YR19

NOT INSTALL

SYSCLK_INP8 YR18
 SYSCLK_INN8 YR20

NOT INSTALL

PA_EXP_A_RXP[0..7] >>> PA_EXP_A_RXP[0..7] [42]
 PA_EXP_A_RXN[0..7] >>> PA_EXP_A_RXN[0..7] [42]

PA_EXP_A_TXP[0..7] >>> PA_EXP_A_TXP[0..7] [42]
 PA_EXP_A_TXN[0..7] >>> PA_EXP_A_TXN[0..7] [42]

PA_EXP_A_RXP[8..15] >>> PA_EXP_A_RXP[8..15] [41]
 PA_EXP_A_RXN[8..15] >>> PA_EXP_A_RXN[8..15] [41]

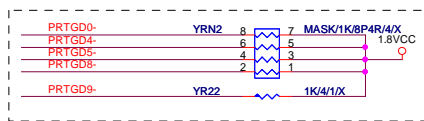
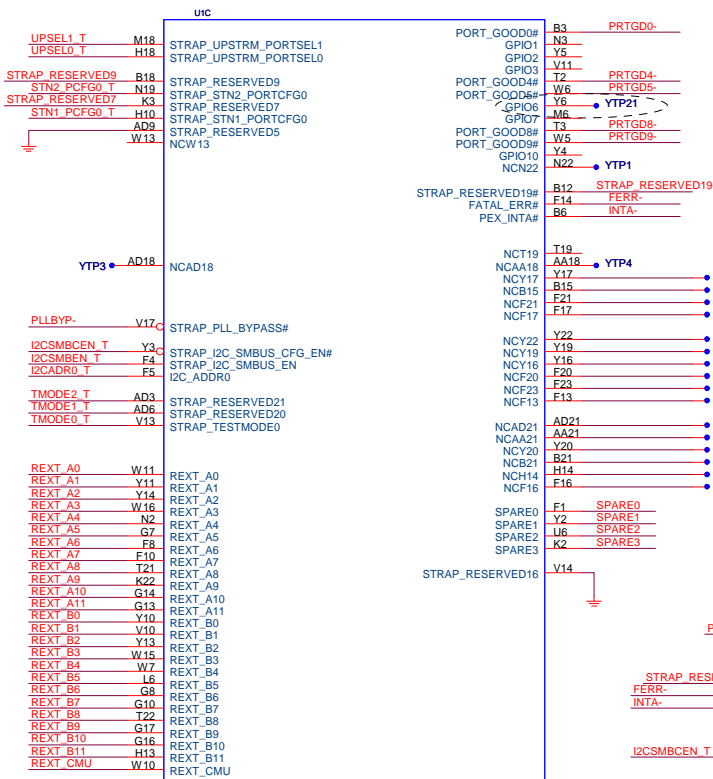
PA_EXP_A_TXP[8..15] >>> PA_EXP_A_TXP[8..15] [41]
 PA_EXP_A_TXN[8..15] >>> PA_EXP_A_TXN[8..15] [41]

PB_EXP_B_RXP[0..7] >>> PB_EXP_B_RXP[0..7] [44]
 PB_EXP_B_RXN[0..7] >>> PB_EXP_B_RXN[0..7] [44]

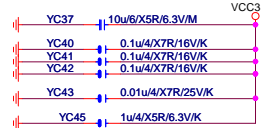
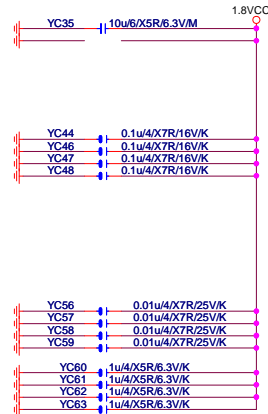
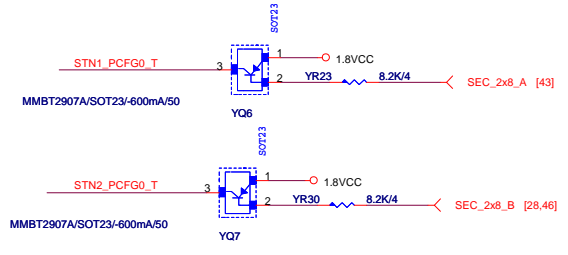
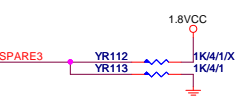
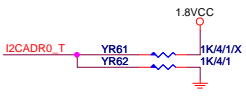
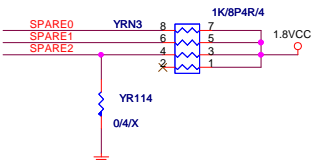
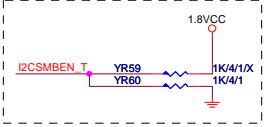
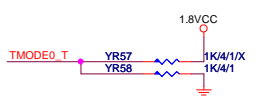
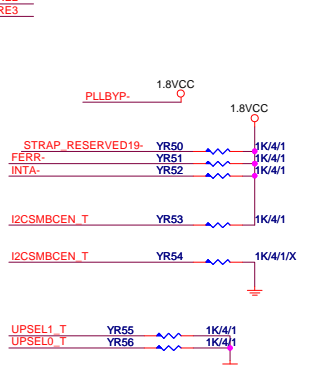
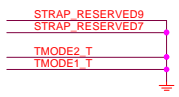
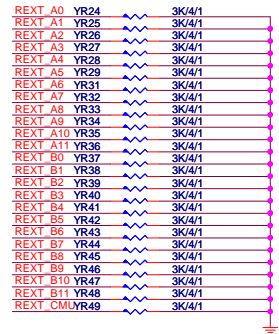
PB_EXP_B_TXP[0..7] >>> PB_EXP_B_TXP[0..7] [44]
 PB_EXP_B_TXN[0..7] >>> PB_EXP_B_TXN[0..7] [44]

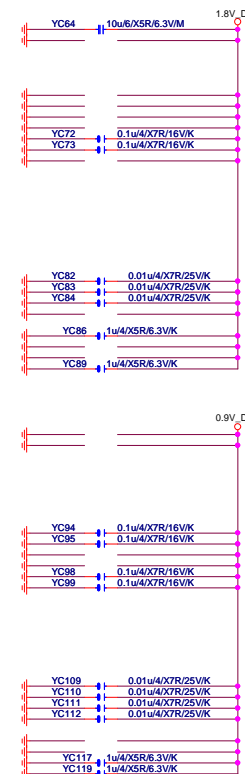
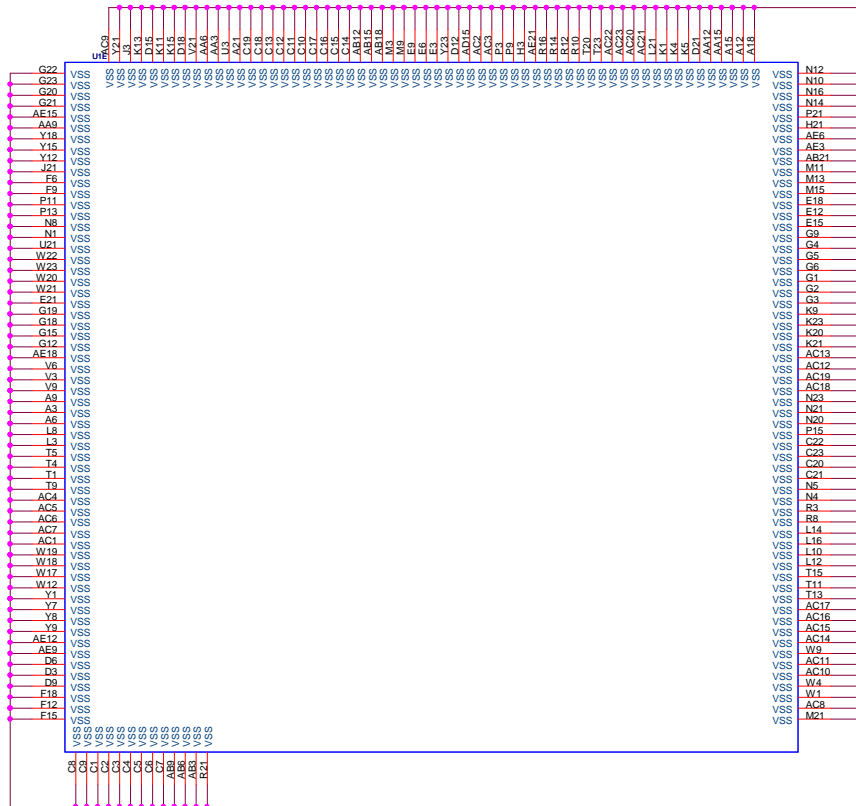
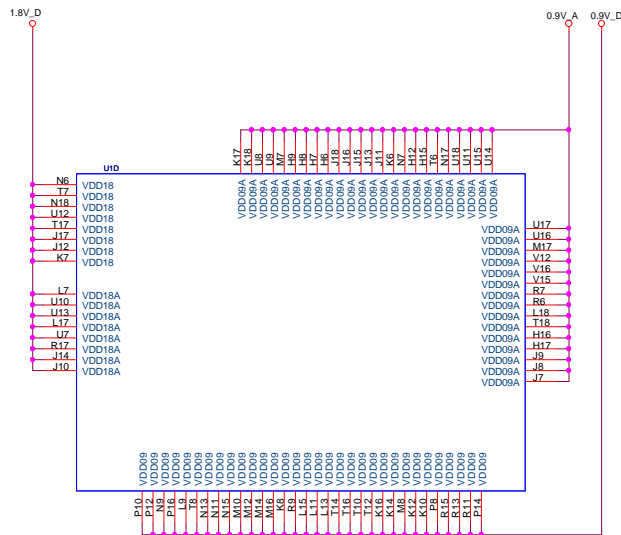
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 PB_EXP_B_RXN[8..15] >>> PB_EXP_B_RXN[8..15] [45]

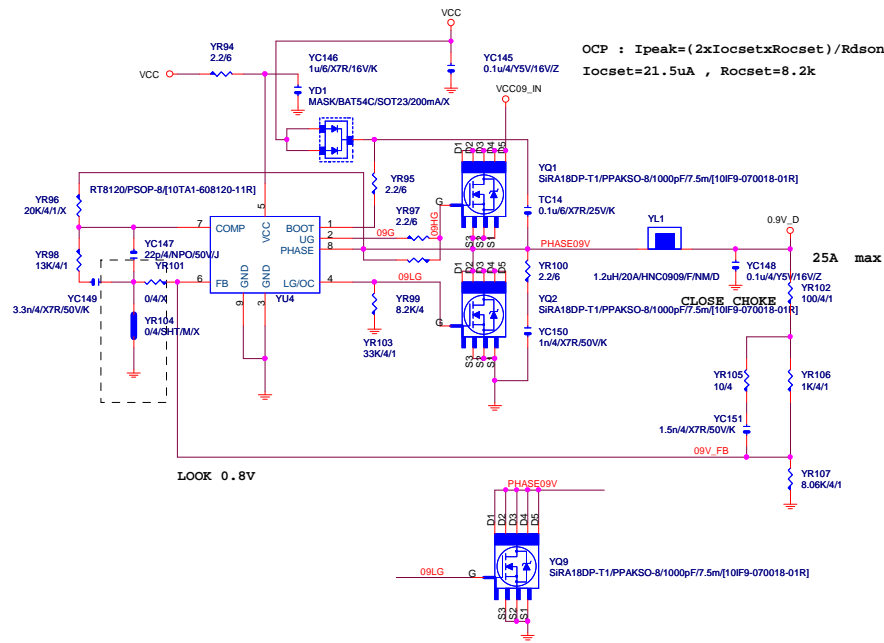
PB_EXP_B_TXP[8..15] >>> PB_EXP_B_TXP[8..15] [45]
 PB_EXP_B_TXN[8..15] >>> PB_EXP_B_TXN[8..15] [45]



Resistors should be placed close to U1

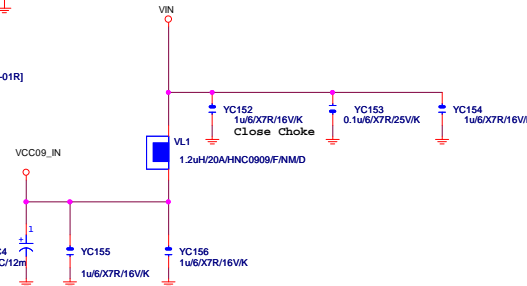
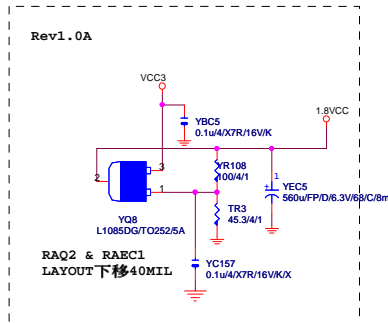
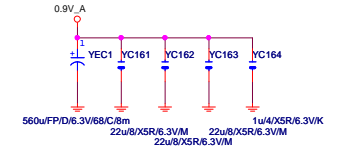
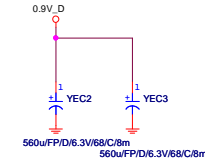
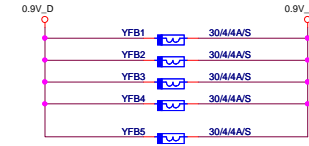




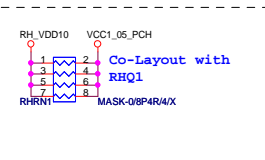
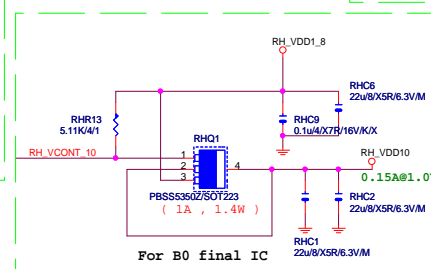
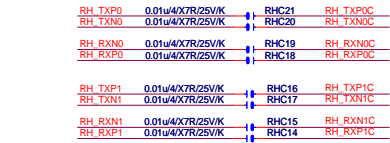
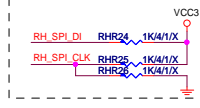
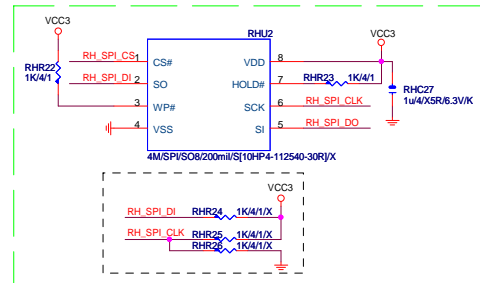
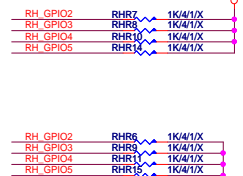
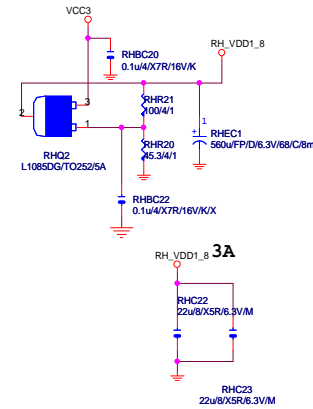
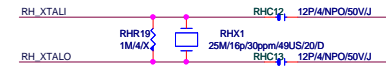
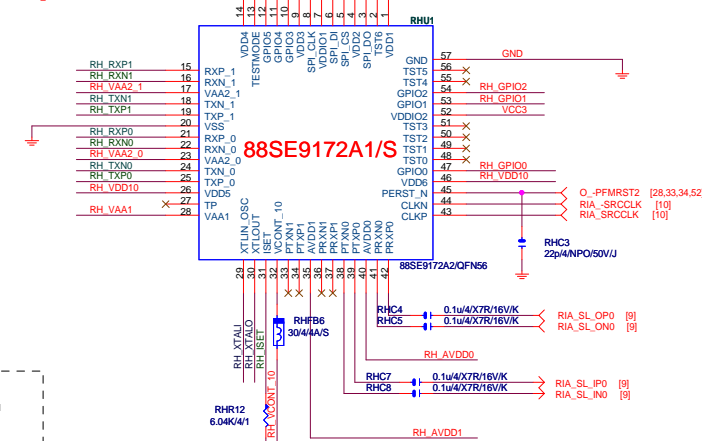
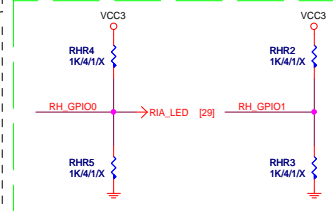
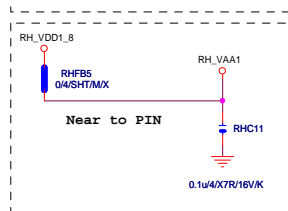
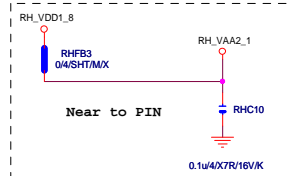
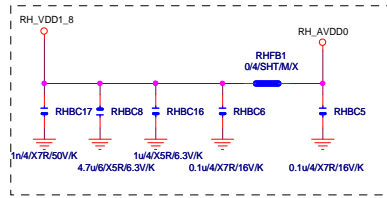
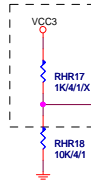


$$OCP : I_{peak} = (2 \times I_{ocset} \times R_{ocset}) / R_{dson}$$

$$I_{ocset} = 21.5uA, R_{ocset} = 8.2k$$



Gigabyte Technology			
Title			
Marvell 9172 -2			
Size	Document Number	GA-Z97X-Gaming G1	
Custom			
Date:	Wednesday, March 05, 2014	Sheet	52 of 54
			Rev 1.0

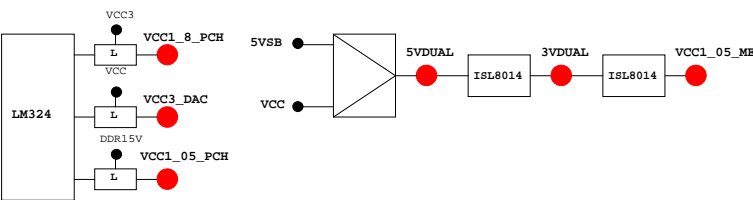


灰色
connector

PIN NAME	PWR	AFTER PIRQ#	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	EN_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/FCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



The diagram illustrates a 16-processor system architecture. At the center is a large box labeled **CPU**. To its left is a box labeled **PCH**. To the right of the CPU, there are two vertical columns of processor blocks. The left column contains six blocks labeled PH1, PH2, PH3, PH4, PH5, and PH6 from top to bottom. The right column contains six blocks labeled DL1, DL2, DL3, DL4, DL5, and DL6 from top to bottom. A horizontal line labeled **VTT** runs along the top of the processor blocks. A vertical line labeled **VCORE** runs along the right side of the processor blocks. The PCH is connected to the CPU and the VTT line.

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH